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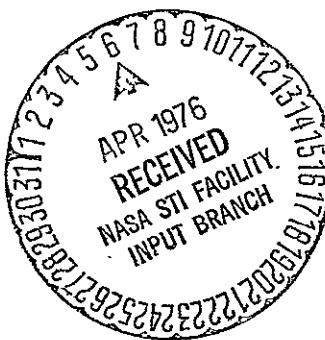
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# DIGITAL CORRELATION DETECTOR FOR LOW-COST OMEGA NAVIGATION

by

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## FOREWORD

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## I. BACKGROUND INFORMATION

A. Statement of the Problem. Omega is a global navigation network which will, when completed, be comprised of eight ten-kilowatt stations around the world. [1,2,3] These stations transmit very low-frequency (VLF) sinusoids in a time-multiplexed format, each transmitting for about one second out of every ten on each of three frequencies. Position is determined by measuring the phase of these signals with respect to each other. The basic problem with making this phase measurement is that the signals are often weak and masked by impulse noise.

To overcome this problem, Omega receivers typically employ a correlation device, or phase-locked loop (PLL), to recover the phase information from the noisy signal. The PLL configuration used in an Omega receiver is most critical to the accuracy and cost of the system since it determines both the quality and format of the inputs to the navigation processor. A look at presently available receivers such as the Tracor, Dynell, and Micro models [4] reveals a wide variety of PLL designs. With all of these PLL configurations available to the Omega designer, a question which arises is whether there is any one optimal PLL design where "optimal" refers to simple configuration, minimal maintenance, good performance, and convenient interfacing.

The purpose of the research presented in this thesis is to develop techniques to lower the cost of using Omega, specifically in the area of phase-locked loops. The design that has been accepted as being "optimal" is called the memory-aided phase-locked loop (MAPLL) since it allows operation on all eight Omega time slots with one PLL through the implementation of a random access memory (RAM).

The first and second chapters of this paper are devoted to a description of the receiver front-end and the signals that it presents to the PLL. A brief statistical analysis of these signals in Chapter II allows a rough comparison of the front-end presented in this thesis to a commercially available front-end to be made. Chapter III describes the hardware and theory of operation of the MAPLL, ending with an analysis of data taken with the MAPLL. Chapter IV lists some conclusions about the system as well as recommendations for possible future work.

The Omega system operates at three harmonically related frequencies: 10.2, 11.33..., and 13.6 KHz. The 10.2 KHz frequency alone has shown itself to be adequate for navigation during several test flights<sup>[5]</sup>; however, it may be desirable to use more than a single frequency to minimize the probability of an ambiguity problem. The PLL to be presented can operate at all Omega frequencies, although for convenience only the 10.2 KHz case will be described.

The Omega sensor processor presented here is working as described and has provided good sensor processor data on several test flights.

B. Description of the Receiver Front-End. Before anything can be said about signal processing, some time should be devoted to the equipment that recovers the signals off the air. This section is devoted to a description of the components that provide the signals to the PLL. A block diagram for these components is shown in Figure 1. The signals from the antenna receive slight amplification in the preamplifier and are fed into the front-end where they are highly filtered and hard-limited. The front-end has two outputs: a threshold

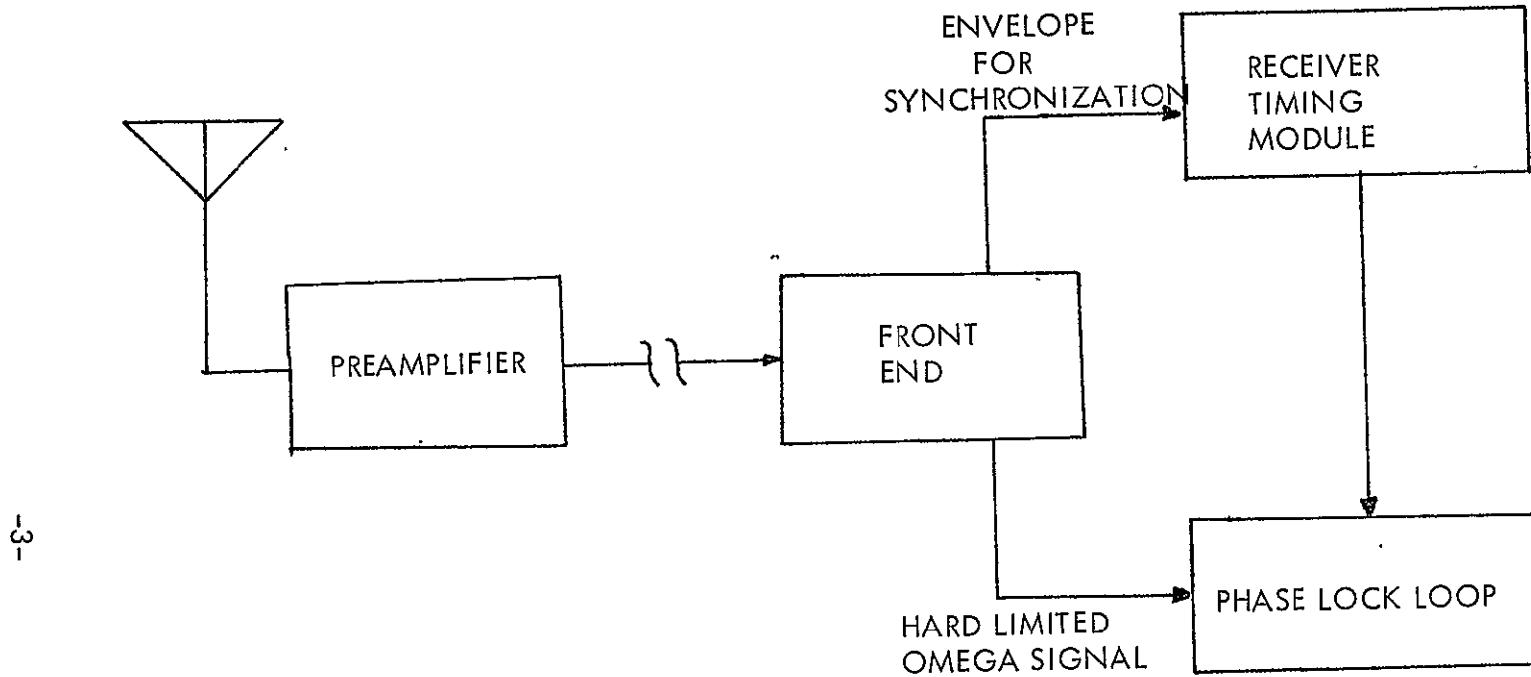


Figure 1. Block Diagram of Components that Provide Signals to the PLL.

detected signal envelope to allow the receiver timing unit to start on the strongest station, and a hard-limited, TTL-compatible signal representing the Omega zero crossings. The input to the front-end is analog, and its outputs are digital.

Since this thesis deals with the PLL, in-depth descriptions of the front-end equipment will not be given, although complete details have been published by Burhans. [ 6,7 ]

1. Antenna and Preamplifier. A short whip or wire antenna is by far the simplest to install but suffers from locally-generated precipitation static in snow or rain, and is non-directional with respect to nearby thundershower spherics and other local interference. A loop or crossed pair of loops can reduce local noise in many applications but requires more processing for the phase ambiguity introduced depending upon the bearing of the transmitting source. Much work has been done and many methods are proposed for reducing antenna noise problems [ 8 ], all of which tend to increase the cost of present receiver systems. Since the goal of this research emphasizes low-cost, a 6 meter wire was used for these tests. The effective height of that antenna after the preamplifier as seen by the front-end is one meter.

The purpose of the preamplifier is to match the high impedance of the antenna to the low impedance of the front-end input while supplying sufficient gain to overcome losses incurred during the impedance transformation. The high impedance input to the preamplifier is accomplished by using a MOSFET and the low impedance output by a small audio transformer. The phase shift through the preamplifier is negligible.

2. Front-End and Envelope Detector. The purpose of the front-end is to amplify the wideband signal from the preamplifier and pass only the frequency of interest (10.2 KHz) to the PLL. This is accomplished by feeding the wideband signals into split-ring ceramic filters, which act like mechanically-tuned tuning forks. These devices have a very high Q and are potentially available at low-cost, if sufficient demand can be created. After the first bandwidth reduction stage, the signal is amplified and low-pass filtered (at 4 to 5 times the center frequency) to remove some of the spurious high-frequency response of the ceramic filter network. The signal is further reduced in bandwidth by being fed into another ceramic filter network. The resulting bandpass curve is shown in Figure 2. Again, the phase shift through this network is negligible. The signal is then limited through a commercially available F.M. limiter-detector integrated circuit. The limiter is followed by a TTL-compatible hard-limiter and the signal is fed to the PLL. The overall gain from the antenna input to the limiter output is around 100 dB.

The detector output from the limiter-detector integrated circuit is a voltage that represents the envelope strength of the carrier. The curve showing the relationship between front-end input to detector output is shown in Figure 3. This data was obtained by inputting a signal of known strength into the front-end and monitoring the detector output. Since the preamplifier makes the antenna appear to have an effective height of one meter, the signal strength of a signal resulting in X microvolts at the output of the preamplifier is X microvolts/meter.

Figure 4 shows typical signal strengths for several Omega stations. The solid lines represent measurements taken in New York<sup>[9]</sup> with a 30 Hz bandwidth

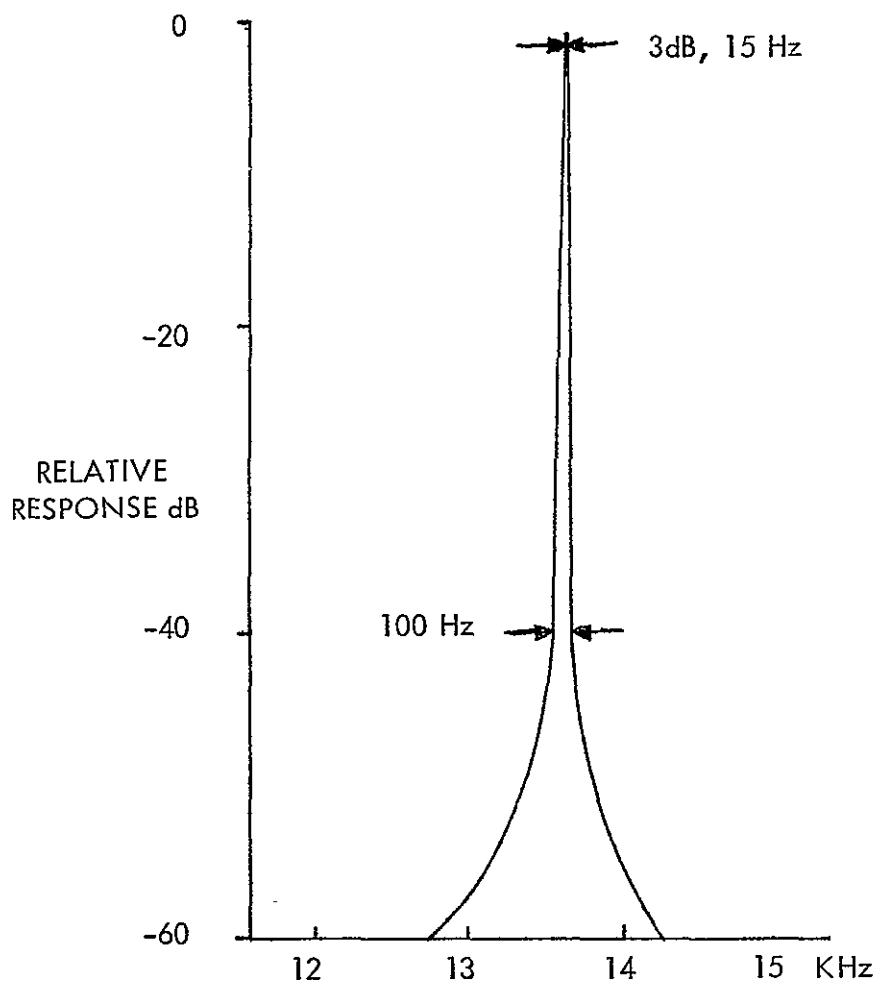


Figure 2. Two Stage Filter.

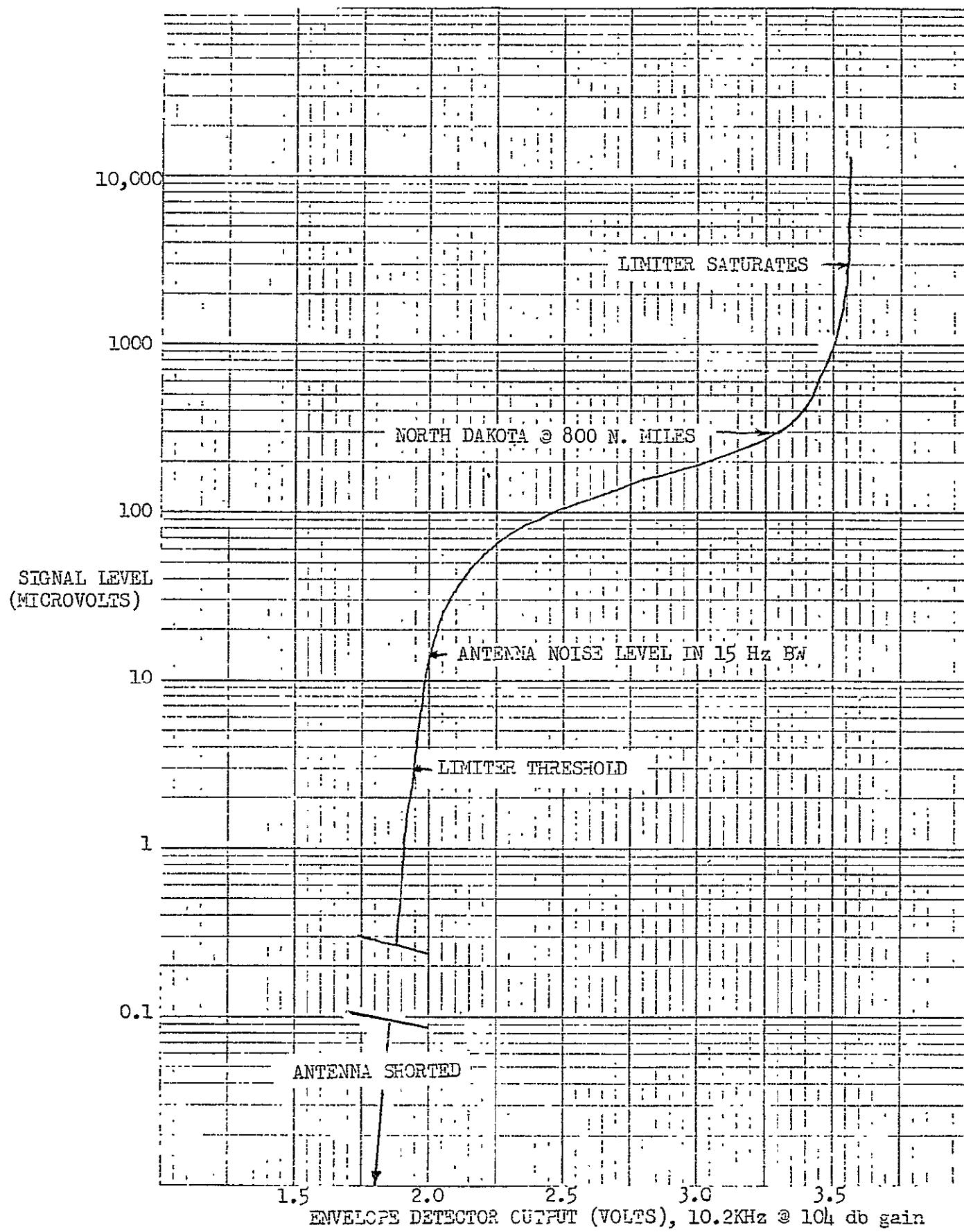


Figure 3. Envelope Detector Characteristics

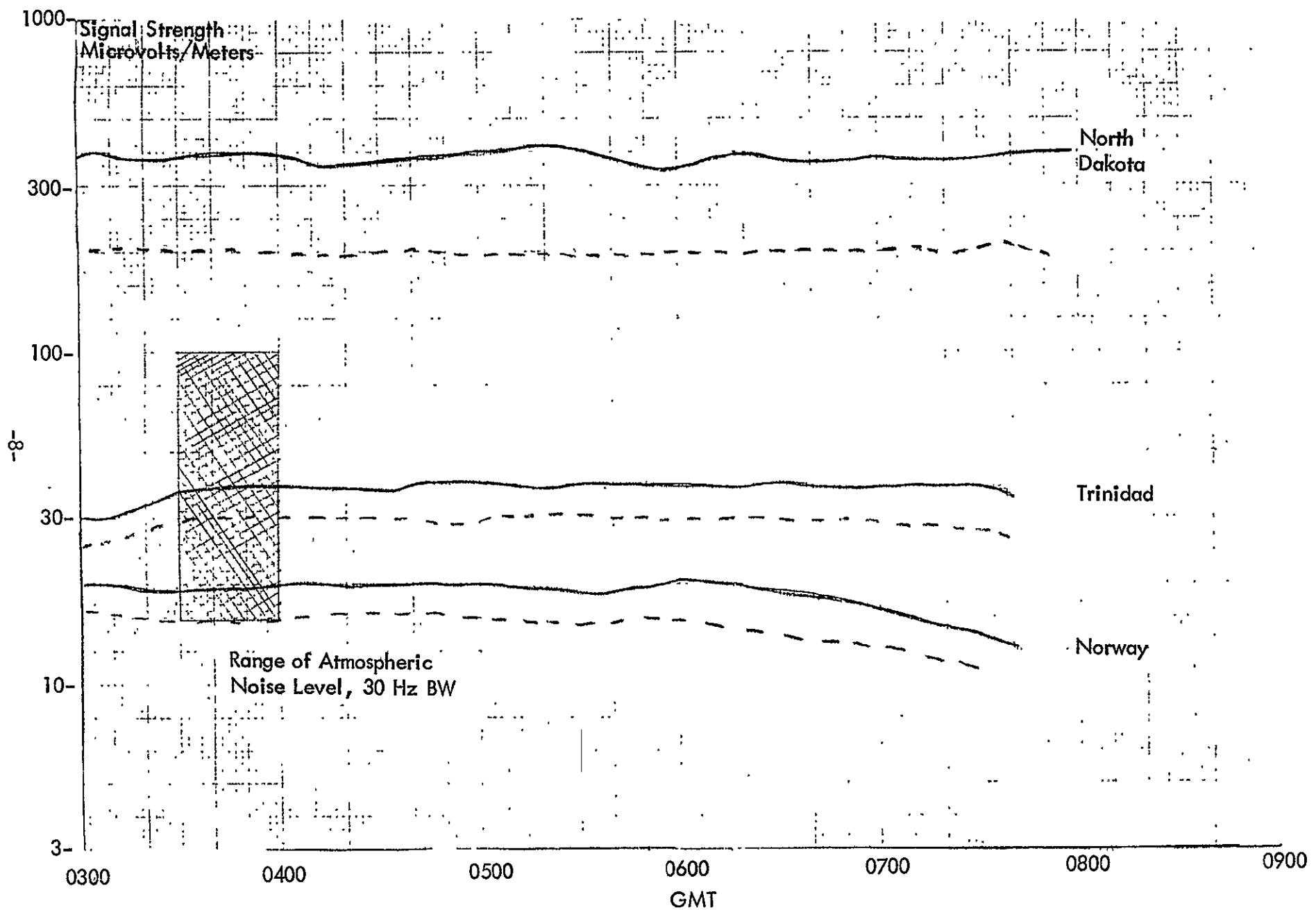


Figure 4. Omega Signal Strength.

receiver and the dotted lines represent measurements taken with a commercially available receiver (100 Hz bandwidth) in Athens, Ohio with an antenna system similar to that used for the system being described here. The purpose of presenting this data is to show that the signal levels detected by the front-end being described and by commercially available receivers are quite similar. Although only two points of comparison can be noticed between Figures 3 and 4, the level of the North Dakota station and the noise level, the three station information of Figure 4 was included as an indication of the large variety of signal strengths that a system would have to cope with.

The above implies that the signals produced by the receiver front-end used for this thesis and a commercially available front-end are roughly the same, which tends to indicate that the results to be shown later in this thesis have not been enhanced or degraded by an exceptional receiver front-end.

### C. Preliminary Analysis.

1. Test Configuration for Phase Averaging. When this research into the development of a low-cost Omega receiver first began, one idea that seemed promising and quite simple to accomplish digitally was to measure the phase of each carrier cycle with respect to a local clock and numerically average it for the duration of the Omega time slot (nominally one second). The setup for making this measurement is shown in Figure 5. The 10.2 KHz reference clock turns on an edge-triggered D-type flip-flop whose high Q output allows clock pulses at  $64 \times 10.2$  KHz to be fed into a divider. The clock pulses stop going to the divider when the Omega signal at 10.2 KHz arrives, since this signal is connected to the CLEAR of the flip-flop. A  $64 \times 10.2$  KHz clock is used since 64 counts will be accumulated

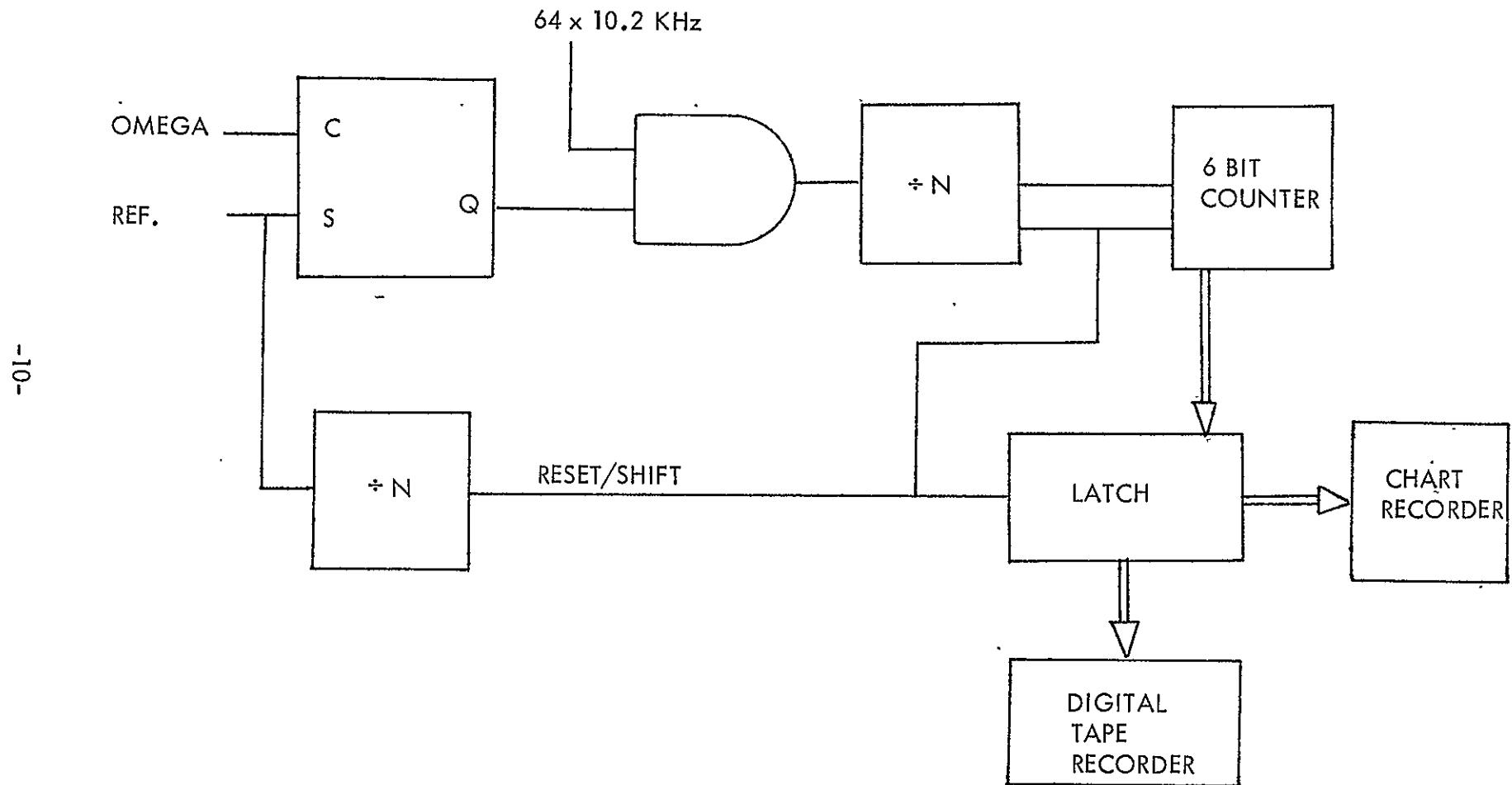


Figure 5. N-Cycle Recording Configuration.

in the divider during one Omega cycle if the phase difference between Omega and the receiver clock is 360 degree. The full range of the phase differences then can be handled by a 6-bit counter, which can accumulate up to 64 counts. The reference clock also feeds directly a divide-by-N counter. The number N determines how many carrier cycles of the incoming Omega signal will be averaged, since after N cycles have entered the divider, its output will change state causing the averaged data to be shifted to the I/O devices and the counters to be cleared in preparation for the next measurement. The count in the 6-bit counter at the end of the measurement interval represents the averaged phase, since the sum of N sets of data (representing N phase measurements) has been divided by N and placed in that counter. The value of N chosen for these tests is  $2048 \times 3$ , which is easily realized and is within the measurement interval constraint. The time required to make this measurement is  $N/10.2 \text{ KHz} = 6144/10.2 \text{ KHz} \text{ or } 602 \text{ ms}$ .

The above process is synchronized with the time-multiplexed Omega by gating signals from the receiver timing system (not shown).

Data taken with this circuit configuration is shown in Figures 6 and 7. Figure 6 shows the strongest station, North Dakota (time slot D), with respect to an offset reference being measured by both the averaging receiver and the Tracor 599-R. Although the Tracor's trace is considerably cleaner, the averaging receiver would provide a navigable output if all stations were as powerful as North Dakota. However, as can be seen in Figure 7 which shows Trinidad (channel B), the trace is so noisy as to be of little use for navigation. It should be mentioned that the day these measurements were taken was an electrically "clear" day, i.e., low

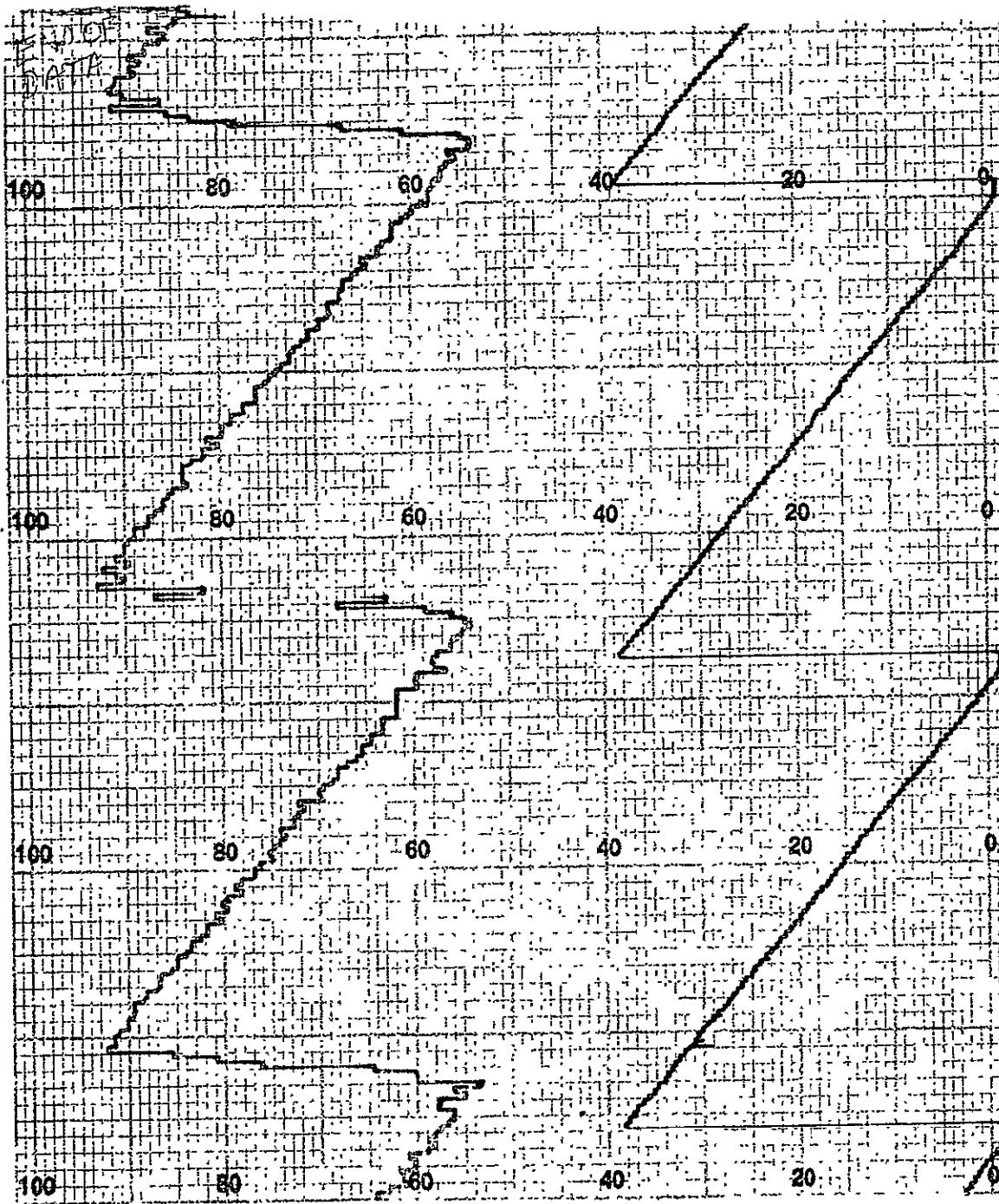


Figure 6. North Dakota (D) Station with Respect to Offset Reference Clock. (2:30PM, July 22, 1974, 5 minutes per inch; upper trace is Ohio University receiver, lower trace is Tracor 599-R).

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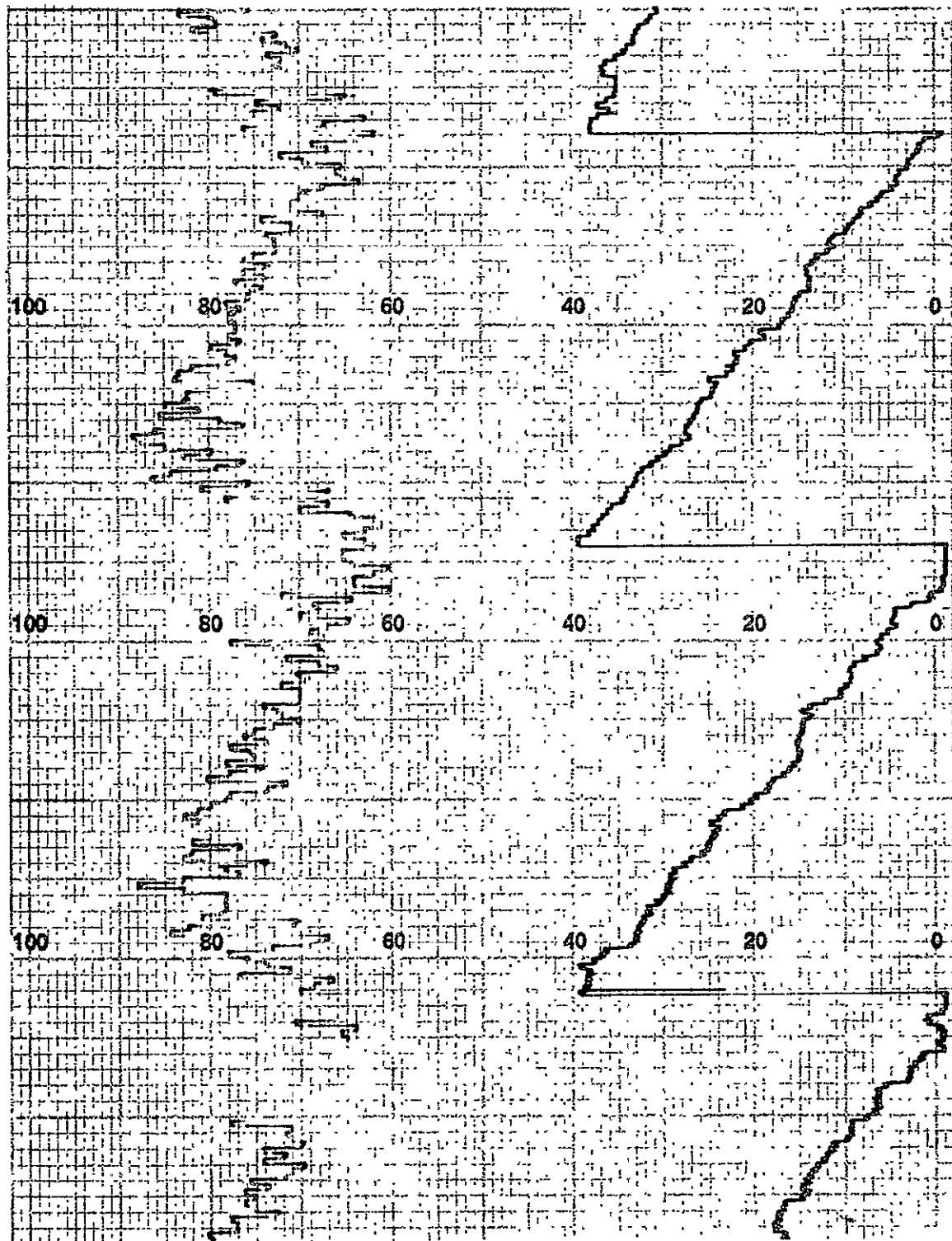


Figure 7. Trinidad (B) Station with Respect to Offset Reference Clock. (9:25AM, July 22, 1974, 5 minutes per inch; upper trace is Ohio University receiver, lower trace is Tracor 599-R).

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atmospheric noise. On a "noisy" day, the Trinidad trace was observed to be completely obliterated.

Based on the results shown in Figures 6 and 7, it was concluded that some form of signal-to-noise ratio enhancement would be needed to provide a navigable signal, which led to the investigation into phase-locked loops.

## II. ANALYSIS OF INCOMING OMEGA SIGNALS

The fact that the phase averaging circuit (Chapter 1, Section C) did not yield the expected results, brought up questions as to the actual statistical properties of the incoming Omega phase. This chapter is devoted to the description of the equipment used to record this phase information and conclusions made from it. These analyses were performed with the intention of estimating the statistical properties of the signals from this particular front-end to provide design guidance for the PLL, and not as an in-depth study. Therefore, any mention of signal-to-noise ratio or any other signal parameters is meant as an estimate and for only one limited period of time.

A. Single-Cycle Phase Measurement. The purpose of this experiment is to sample the instantaneous phase of an incoming Omega signal with respect to a stable local oscillator (a rubidium standard) and put this data on magnetic tape for further analysis. Due to the maximum speed limitations of the magnetic tape recorder, the sample is taken every 30 carrier cycles within an Omega time slot. The phase is recovered digitally as shown in Figure 8.

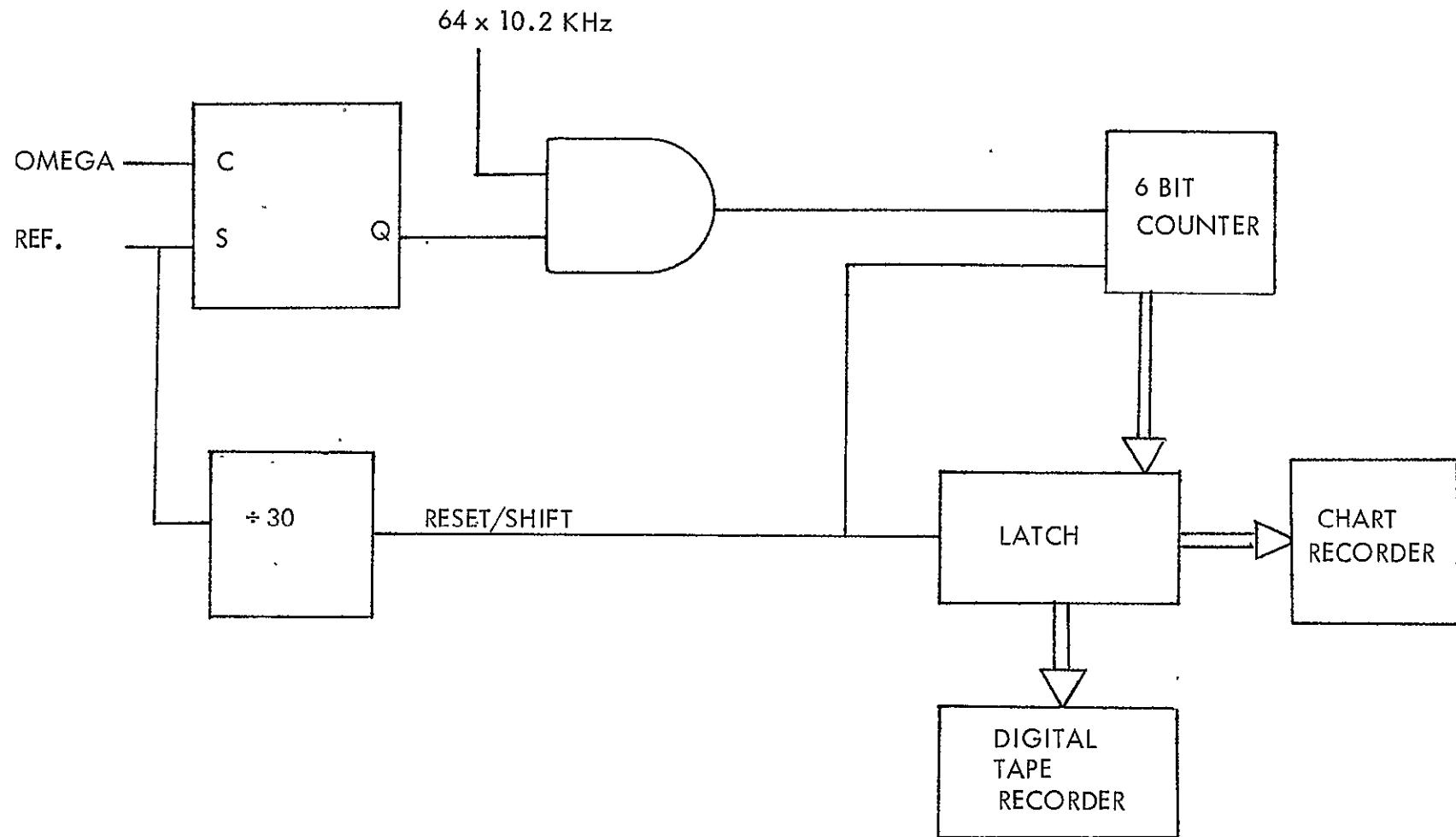


Figure 8. Single-Cycle Omega Phase Measurement.

The digital phase measurement is made in the same way as in Chapter I, Section C, except that in this case the data is sent directly to the I/O devices without averaging.

With the present receiver timing scheme, a gate of 602ms. per Omega time slot is available for measurement which represents  $602 \times 10.2$  KHz or 6140 cycles. Since the measurements are made every 30th cycle, there are 204 samples recorded per time slot.

B. Analysis of Single-Cycle Data. Digital plotter outputs of the data retrieved with the above configuration are shown in Figures 9 and 10. Figure 9 represents the random phase of a clear time-slot (no station transmitting) and Figure 10 represents the phase during one Trinidad (B) time-slot. The clear channel and Trinidad were chosen since Trinidad is typical of a weak signal and the clear channel represents the phase characteristics when no signal is present. This clear channel baseline is useful, since without it the slight correlation in the Trinidad plot is not readily apparent.

The apparent discontinuity of these plots near the 0 and 360 degree points is due to the digital manner in which the data was recovered. If the phase is at 0 degrees at one point and the next phase measurement is 5 degrees less, it will not appear at -5 degrees, but rather at +355 degrees.

These measurements were taken in the mid to late summer, which is a most important factor when dealing with VLF since at low-frequencies the nature of noise is quite different from season to season. In the summer, impulse noise due to lightning is considerably more severe than in winter. The data presented here, then, is of the "worst case" variety.

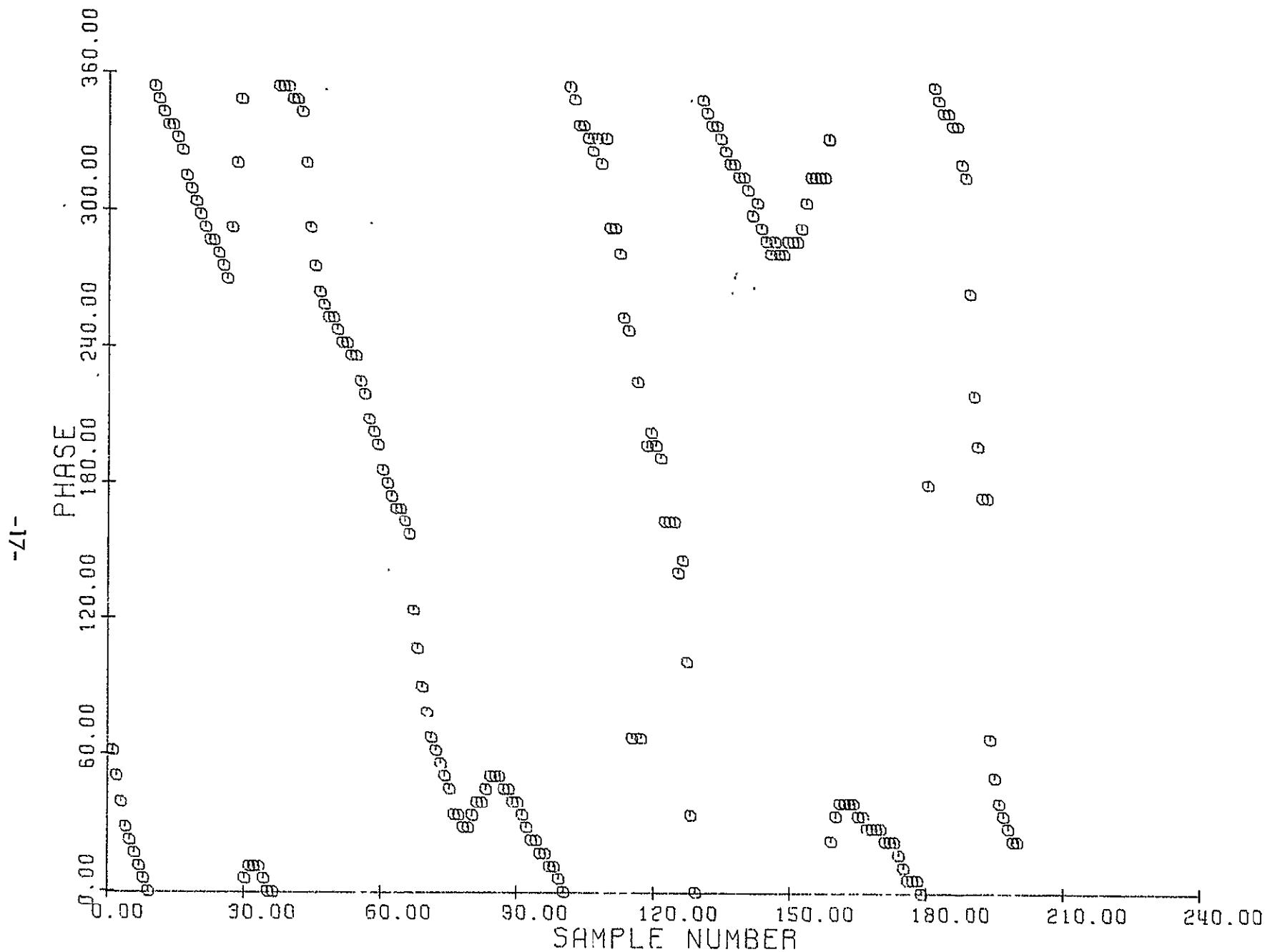


Figure 9. Phase of Sampled Noise in One Omega Time Slot.

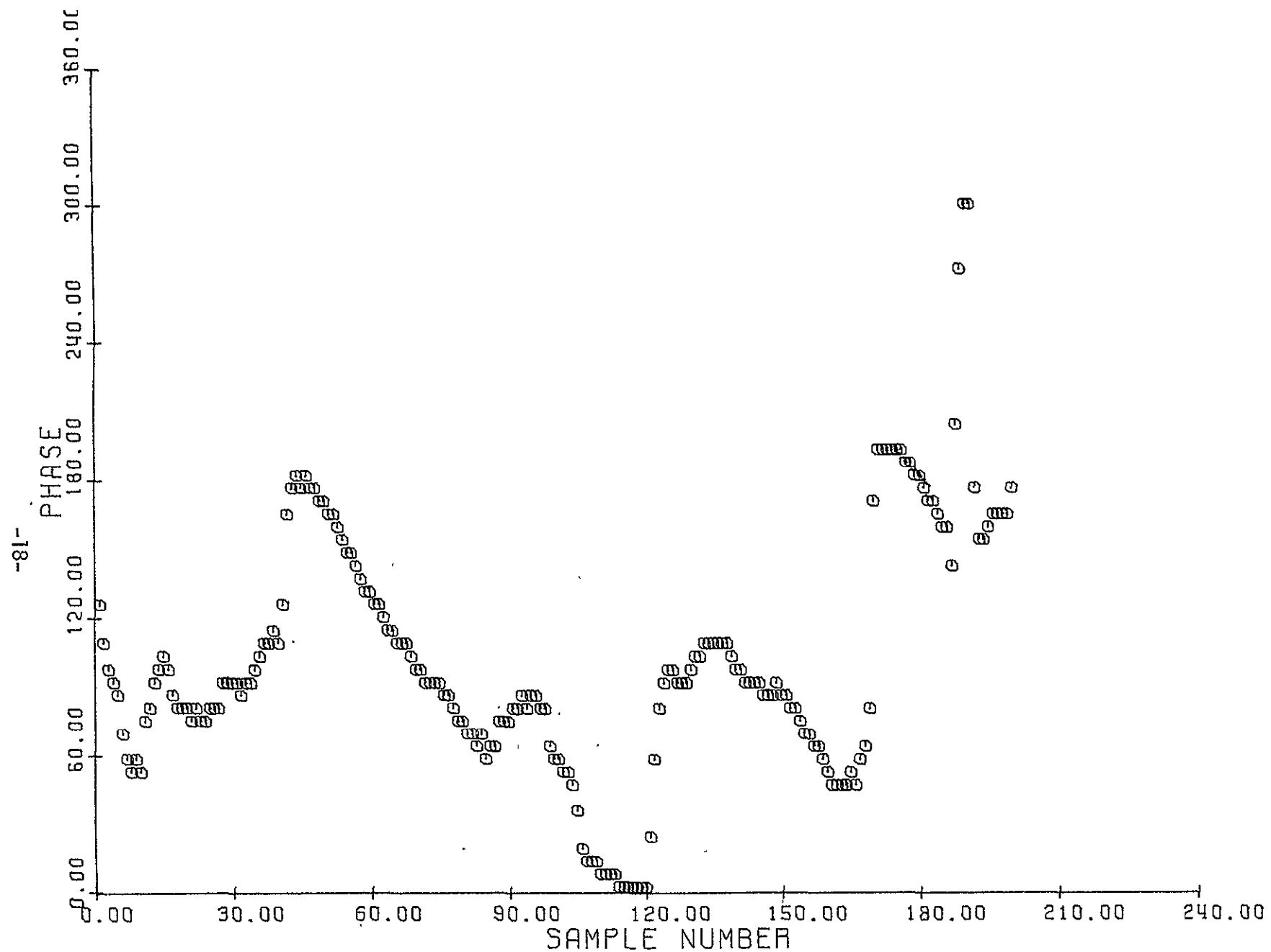


Figure 10. Phase of Omega B Channel for One Time Slot.

Phase distribution information can be determined from the single-cycle data by collecting the data over a number of time slots and plotting the frequency of occurrence of phase at particular points vs. phase. The resulting histogram (a histogram since the data was recovered digitally, i.e., quantized) can then be normalized and compared to mathematical models of phase distributions with known signal-to-noise ratios. Normalization involves arranging the frequency of occurrence scale factor so that the area under the histogram is one. The area under a histogram can be determined if it can be assumed that the probability of the phase surrounding the quantization points is equal to the probability of the quantization points themselves. A Lagrange interpolation polynomial could have been used to determine and normalize the area under the curve, although the method described above is considerably less time-consuming and does provide good results.

Examples of phase distributions taken from single-cycle data are shown in Figures 11 and 12, along with a mathematical model given by Schwartz. [ 10 ] This model is for the phase distribution of a sinusoidal signal in Gaussian noise through a narrow band receiver. The model is applicable except for the fact that the type of noise affecting the Omega phase distribution most is impulse as opposed to Gaussian. The phase distribution of impulse noise is difficult to model since several new parameters are introduced, such as the amplitude, frequency, and duration of the impulses as well as the impulse response characteristics of the network being modeled.

Since impulse noise is difficult to model, [ 11 ] the Gaussian noise model will be used in order to give a rough estimate of the signal-to-noise ratio. The

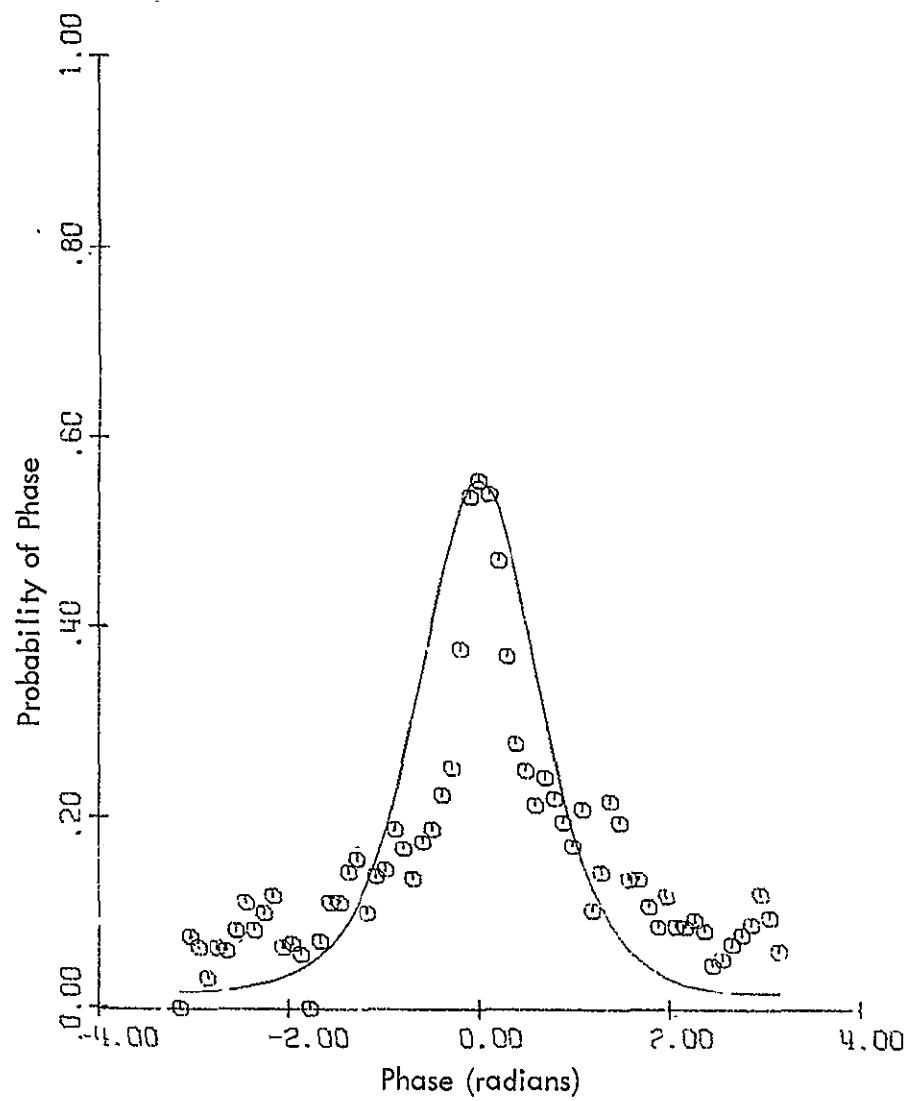


Figure 11. Phase Distribution of the Raw Trinidad Transmission.

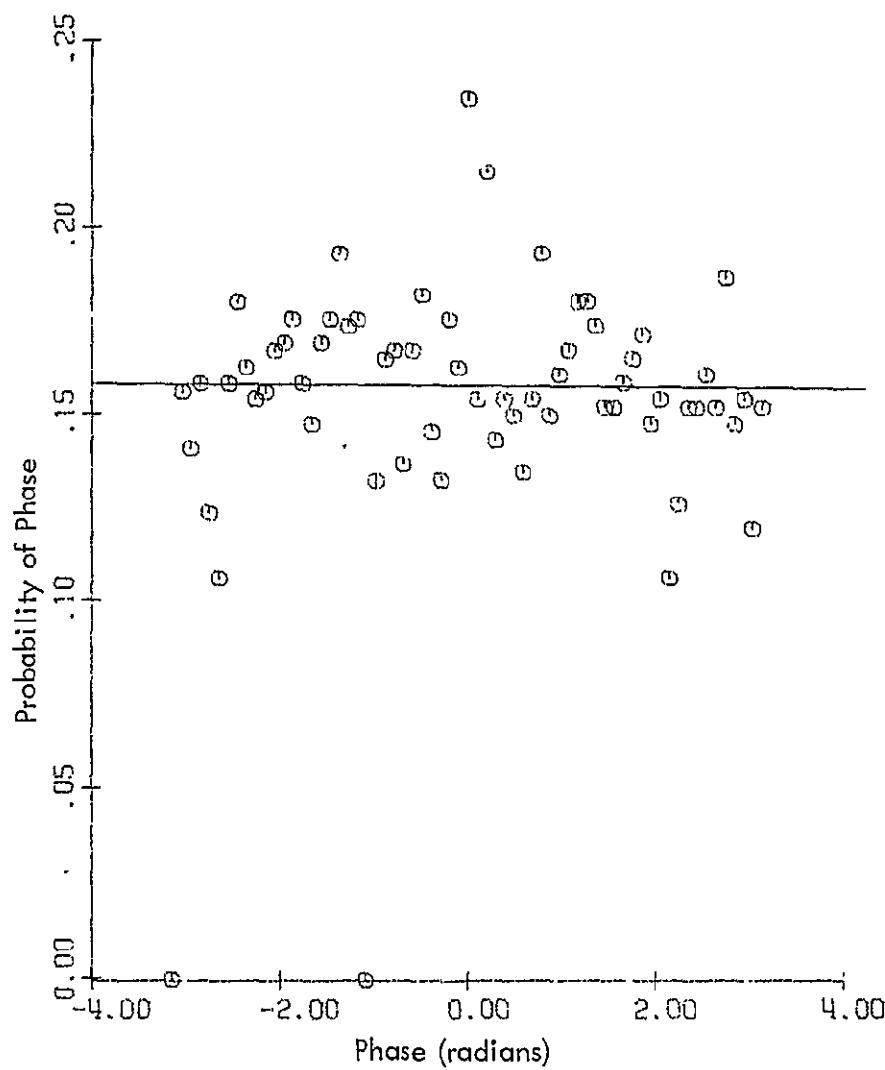


Figure 12. Phase Distribution When No Signal is Present.

model for the probability density function for the phase is represented by the continuous curve in Figures 11 and 12 and is given by the equation:

$$F(\theta) = e^{-S^2/2\pi} + 1/2 \sqrt{S^2/\pi} \cos \theta e^{-S^2 \sin^2 \theta} (1 + \operatorname{erf} S \cos \theta)$$

where  $S^2 = A^2/2N$  = power signal-to-noise ratio.

Figure 11 represents the phase distribution of the Trinidad station derived from single-cycle data accumulated over 14 time slots (14 time slots  $\times$  204 samples/time slot = 2856 samples). The signal-to-noise ratio number used for the model in Figure 11 was 0 dB, which is within the range of values given in the literature. In Figure 11, it can be seen that the peak of the actual distribution is narrower than the Gaussian model, although the skirts of the model distribution are lower. This can be explained by the fact that the receiver will accurately track the phase of the signal (because of its narrow bandwidth) between impulses, but will radically lose track due to the "ringing" of the front-end filters when an impulse arrives. A blanking or editing circuit, which would halt PLL operation when an impulse exceeding a predetermined threshold is detected, is currently being developed for the system which should greatly immunize the system from such impulse noise.

Figure 12 represents the phase distribution when no signal is present which shows that there are no systematic biases in the system or the data processing techniques. The mathematical model for this no-signal case becomes a straight line with a value of  $1/2\pi$  for  $S^2 = 0$ .

Further information can be gained from the single-cycle data by differentiating the phase information with respect to time to determine the frequency components of the signal from the front-end. Since each data point is taken every 30th 10.2 KHz

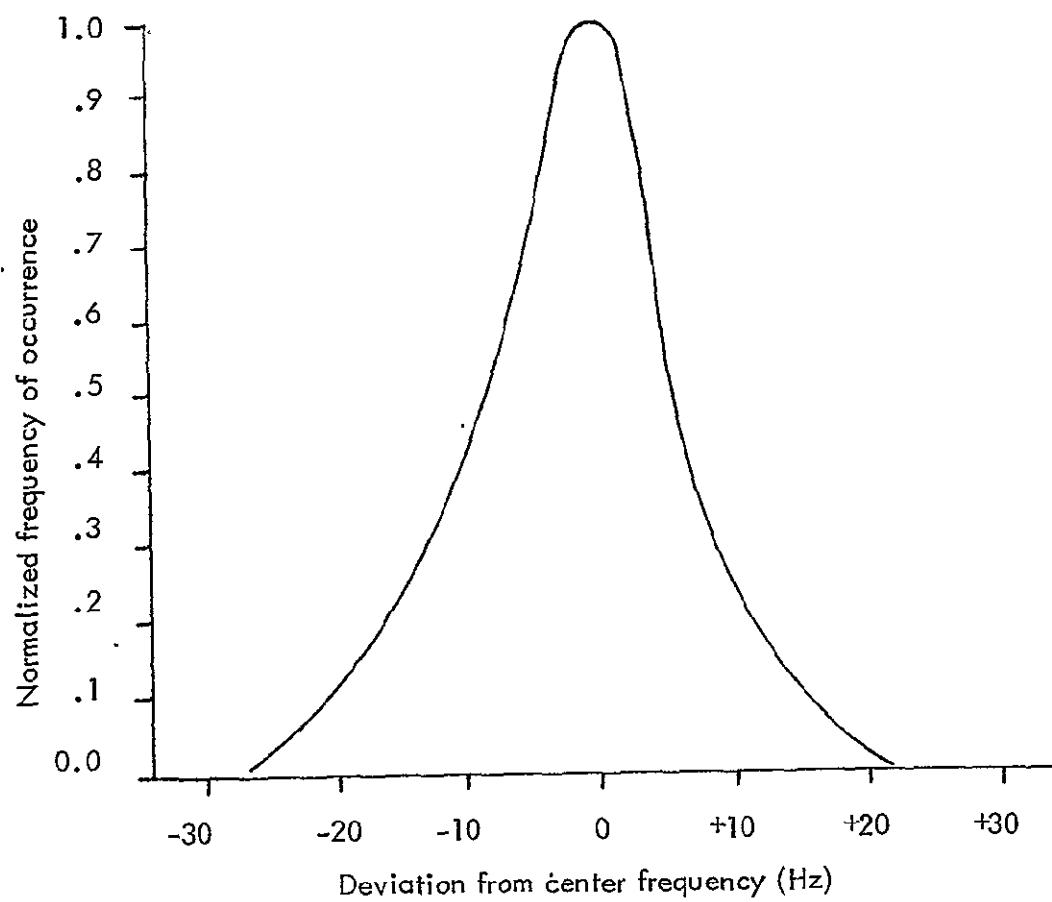


Figure 13. Differentiated Phase Data from the Trinidad Station.

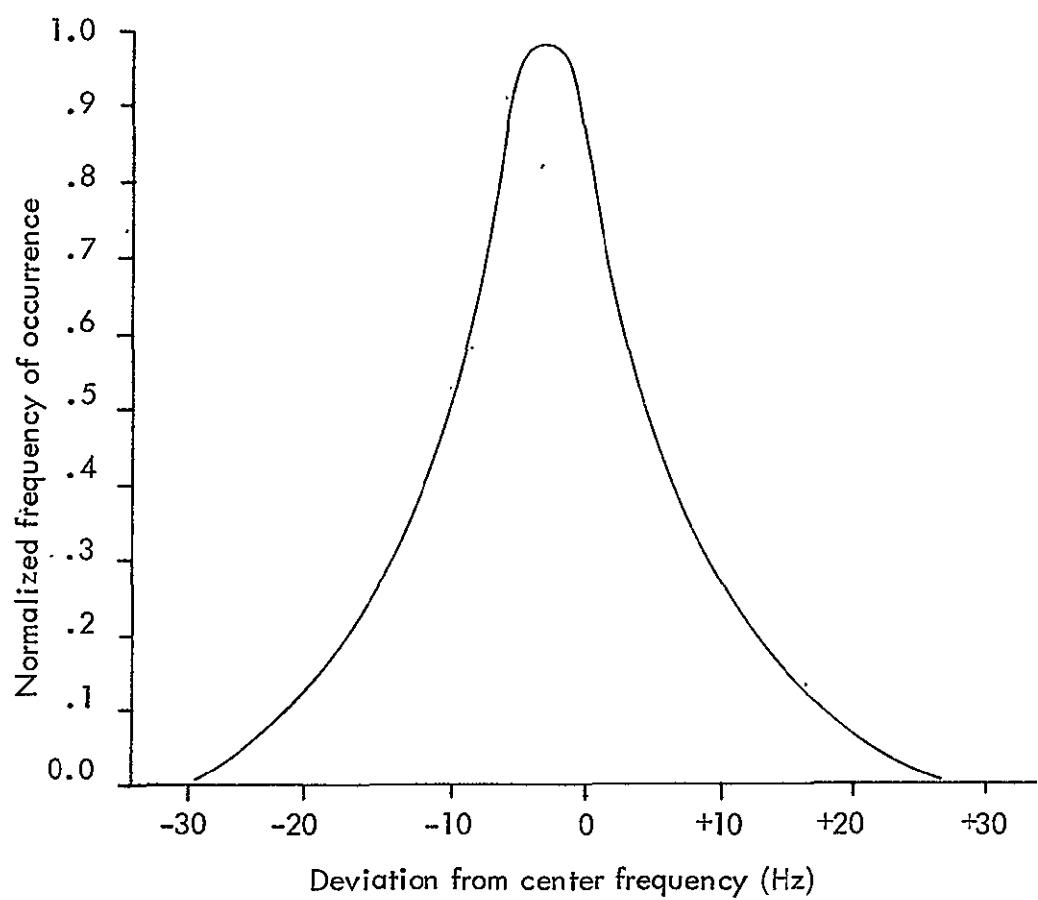


Figure 14. Differentiated Phase Data from the Clear Channel.

cycle, the data points are roughly 3 ms. apart. If, for example, there was a change of phase of 9 degrees between data points, the rate-of-change of phase (frequency) would be .025 cycles/ 3 ms. = 8.33 Hz.

Plots of the Trinidad and clear channel frequency components are shown in Figures 13 and 14, respectively. It is reassuring to note that both curves resemble the bandpass curve of the receiver front-end shown in Figure 2. The fact that the peak of the clear channel frequency distribution is offset is most likely due to sidebands from a local radio transmission or even powerlines (10.2 KHz is the 170th harmonic of 60 Hz).

### III. DIGITAL PHASE LOCK LOOP

A commonly-used signal-to-noise ratio enhancement device is the phase lock loop (PLL). The PLL operates by comparing the phase of a receiver signal to a locally generated signal at the same frequency and adjusting the phase of the local signal until they coincide. A typical first order analog PLL block diagram is shown in Figure 15.

The phase detector has two inputs: a signal off the air and a signal generated by the loop whose phase is to be locked to the phase of the signal off the air. The phase detector output is a voltage proportional to the phase difference of its inputs. In most cases, the phase detector can change its output at a per cycle rate, i.e., its output will change if the phase from one cycle to the next changes.

A low-pass filter, or integrator, is used to slow the rate of change of the phase detector output. In order for the filter output to change, a phase error

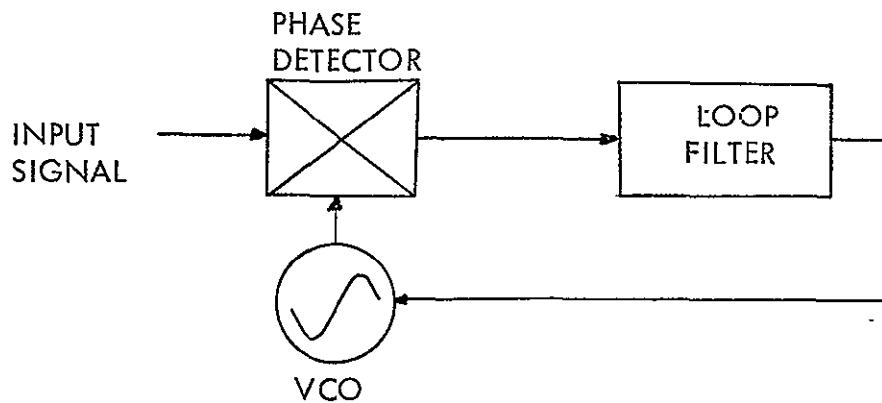


Figure 15. Basic Phase Lock Loop.

must be detected over a number of carrier cycles (the number depending upon the time constant of the filter). This filtering tends to cancel the effects of noise, since the phase deviations resulting from noise are not correlated over a large number of carrier cycles.

The filter output is fed into a voltage-controlled oscillator (VCO) whose center frequency is the same as the frequency of the signal off the air. The VCO will deviate slightly from its center frequency depending upon its input voltage. Since a change in frequency causes a change in phase, phase lock is achieved through proper manipulation of the VCO input.

The loop is closed as the VCO output is fed into one of the phase detector inputs.

The above is a brief description of an analog phase lock loop. Although it has been used successfully for Omega application in the past, it was considered impractical for our low-cost effort for the following reasons: analog

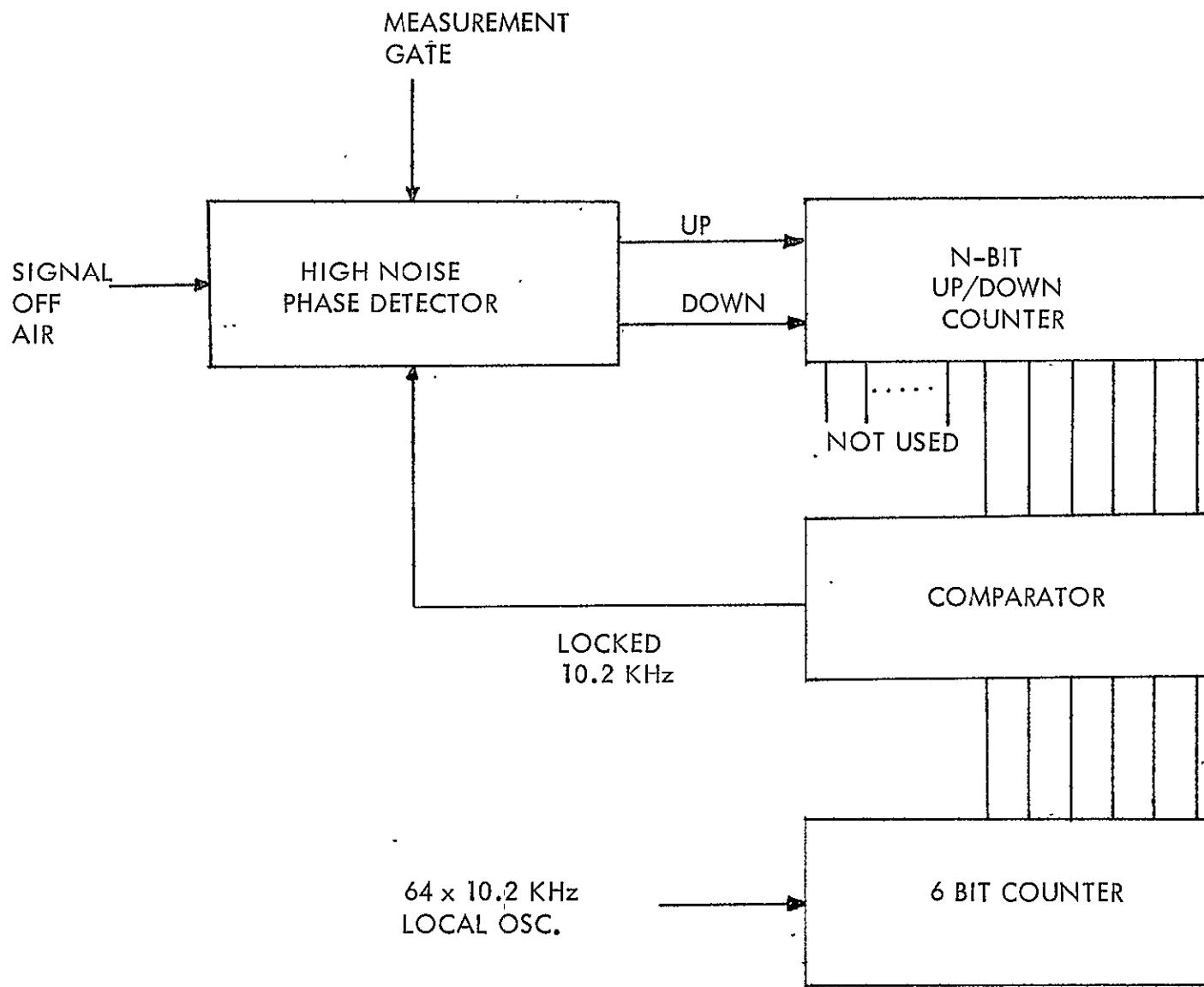


Figure 16. Correlator/Phase Lock Loop Block Diagram.

loops (a) consist of many discrete components (greater expense in fabrication and higher probability of failure), (b) require periodic calibration, (c) require a separate loop for each Omega channel, and (d) do not provide a convenient digital interface.

The above reasons lead to the consideration of a digital phase lock loop (PLL). Many alternatives for the circuit design have been considered. Experimental data taken on a simplest possible PLL [ 12 ] and a study of other proposed Omega receiver methods [ 13, 14 ] have provided insight into the particular digital phase-locked loop design selected here.

A. Basic DPLL Operation. The description to be given here is for one specific loop, although many of the concepts extend to all DPLL's. The block diagram is shown in Figure 16.

As with the analog loop, the phase detector has two inputs: the signal off the air and the locked signal. However, rather than having a single voltage as an output, it has two output lines which feed an up/down counter. The lower order bits of the up/down counter (denoted as "not used" in Figure 16) act as a filter, and the six most significant bits of the up/down counter in the indicated configuration with the comparator and the six-bit counter act as the phase shifter. A more detailed description follows.

1. Phase Detector. A segment of a typical situation that might be encountered by the phase detector is shown in Figure 17. The sporadic position of the Omega signal's positive-slope zero crossings are due to noise, although it is intended that for this interval the Omega signal and the locked signal be in phase. Examining the outputs of the phase detector on a pulse-by-pulse basis

PHASE DETECTOR FOR HIGH NOISE SIGNALS

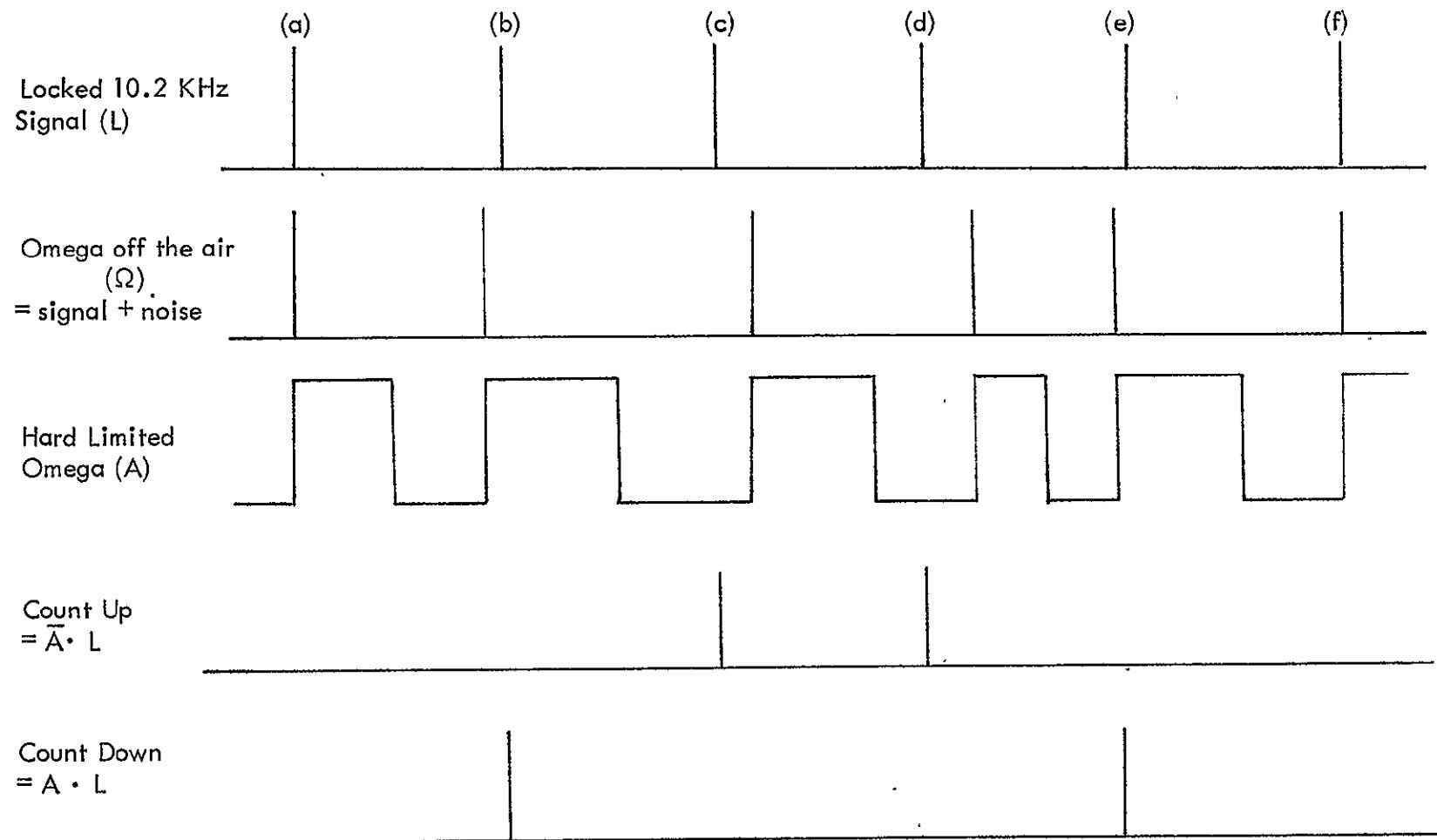


Figure 17. Phase Detector.

yields the following (refer to Figure 17): (a) the pulses are in phase, therefore no output, (b) the locked signal is ahead, so a pulse is fed into the "decrease phase" line, (c) the locked signal is behind and a pulse is fed into the "advance phase" line, (d), (e), (f), etc.

The relative phase of the Omega signal with respect to the locked signal is determined by a window created by the hard-limited Omega signal. If this digital waveform is high when the locked pulse arrives, it means that the locked signal should be retarded in phase in order to achieve phase equality for this particular cycle. Conversely, if the hard-limited Omega wave is low when the locked pulse arrives, the locked signal should be advanced to achieve phase equality or "lock".

The Boolean expression used to describe the logic functions performed by the phase detector are also shown in Figure 17. In the actual circuit these functions are implemented with synchronous logic to prevent illegal states from occurring (such as a simultaneous pulse into the up and down lines).

Note that the phase detector outputs are not proportional to the phase difference, but rather indicate a phase lead or lag on a per cycle basis, i.e., only one decision is made per carrier cycle.

Operation of the loop in this manner makes the loop less susceptible to impulse noise than loops with phase detectors that give outputs proportional to the phase difference. The reason for this is that the perturbations from the true phase caused by impulse noise are quite large as opposed to Gaussian noise. If a proportional phase detector is used, the loop will tend to follow the phase noise variations which is, of course, undesirable.

The statistical information about the Omega signals that was determined from the single-cycle measurements of Chapter II, Section B, tends to verify the above. Specifically, for each time slot, the mode of the phase values, as opposed to the average, more closely approximates the true phase. A proportional phase detector tends to average the phase information since a weighting process takes place. The phase detector presented here performs more of a mode-detection operation since no weighting is applied to the data.

2. Digital Filtering. Filtering, or integration, is achieved by feeding the advance and retard pulses into an up/down counter and using only the six highest order bits for loop control after skipping some of the lower order bits. For example, in the case depicted by Figure 17, the sum of the counts up minus the counts down is zero, implying that no loop control is desired. By skipping two-bits before control, in this case, the locked signal would remain unchanged for that interval. In other words, the number of bits skipped is exponentially proportional to the number of counts accumulated (up or down) before a change is made in the phase of the locked signal. As will be shown in this chapter, Section C, the optimum number of bits skipped for the noisy Omega environment is ten. This means that 1024 correlated zero crossings (the algebraic sum of counts up minus counts down) must be detected before a phase change is made in the locked signal. It should be pointed out that during the 625 ms. measurement interval currently implemented for the Omega receiver, over 6000 zero crossings are measured (10.2 KHz x 625 ms. = 6375 cycles) which means that up to six increments in the loop phase could be made in one Omega time slot.

3. Digital Phase Shifting and Clock Stability. One of the major differences between the analog and digital PLL is the method by which the phase of the locally generated signal is changed. In the analog case, the frequency of the VCO is raised or lowered around the center frequency in order to alter the phase. However, in the digital PLL the frequency of the local oscillator remains unchanged. In fact, for the purpose of this discussion, the local oscillator can be thought of as being absolutely stable.

The phase shift circuit configuration is shown in Figure 18 with the comparator represented by its combinational logic equivalent. The comparator is comprised of one 6-input AND gate and 6 EX-NOR gates. The EX-NOR gate output will be at logical one if both inputs are equal. The AND gate output, which is the comparator output, will be at logical one if all six of its inputs are at logical one. Therefore, the comparator output will be at logical one if the binary number in the six-bit counter is equal to the count in the up/down counter.

The six most significant bits in the up/down counter change very slowly (a maximum of one bit every 1024 cycles) since they are preceded by ten unused bits. The count in the six-bit counter cycles at a 10.2 KHz rate since it is fed by a  $64 \times 10.2$  KHz clock, i.e., a six-bit counter divides by 64, so the counter will count from 0-63 every 10.2 KHz interval.

If the count in the up/down counter does not change, the six-bit counter and the up/down counter will be coincident at a 10.2 KHz rate. The output of the comparator then will be a pulse 1/64th of a 10.2 KHz cycle wide (since the six-bit counter is changing at  $64 \times 10.2$  KHz) and, again, occurring at a 10.2 KHz rate.

10.2 KHz.  
VARIABLE PHASE

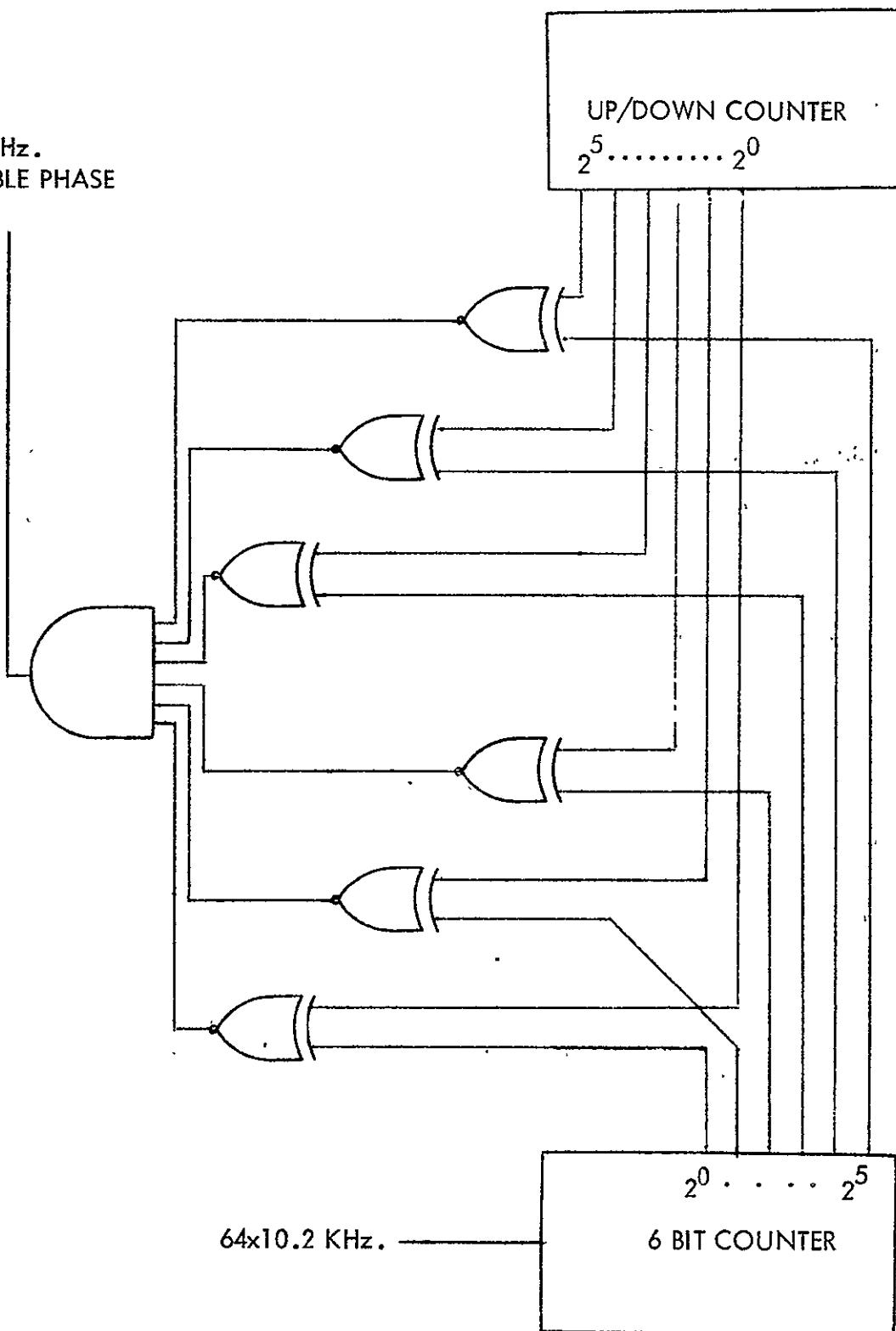


Figure 18. Digital Phase Shifter.

Now, if the count in the up/down counter is incremented by 1024, the pulse coming out of the comparator will occur 1/64th of a cycle later than the previous pulse since the six-bit counter will have to count up by one more in order to achieve coincidence with the up/down counter. The phase can similarly be decreased by lowering the count in the up/down counter.

The comparator output is fed into the phase detector, thus the loop is closed.

The count in the up/down counter represents the phase of the signal that the loop is locked to with respect to the local clock. If the count in the up/down counter is 20, it means that the locked signal lags the local clock by 20/64ths (or leads by 44/64ths) of a cycle.

If the local oscillator were absolutely stable, the number in the up/down counter would represent the true phase of the incoming signal. If this were the case, the loop could be used for range-range navigation.

However, absolutely accurate frequency standards are expensive, making them inappropriate for this application. Hyperbolic navigation eliminates the problem of small clock errors since the lines of position (LOP's) are determined by subtracting the phases of two stations. When the subtraction occurs, only the desired information is left since the local clock drift is subtracted out.

There is, of course, a limit to the amount of local oscillator drift that can be compensated for. Recalling that the Omega signal for each Omega station is present for about one out of every ten seconds, the local oscillator must not drift more than the loop is able to recover between measurements when the loop is physically stationary. When the loop is moving, as it would be when being used

for navigation, the change of phase due to motion plus the clock drift might displace the phase of the locked pulse to such a degree that the loop would not be able to recover during the next Omega transmission. The above led to the constraint placed on the local oscillator which is that it drift not more than the measurement accuracy of the loop (1/64th of a 10.2 KHz cycle) in ten seconds. Fortunately, temperature compensated crystal controlled oscillator (TCXO) packages are available at low-cost that surpass the above criterion.

B. Analysis of Loop Performance. The first version of the PLL was constructed in such a way that the number of bits not used on the up/down counter could be varied from zero to ten. By doing this, data could be taken with the loop using varying filter constants to determine the optimal circuit configuration. Data was taken with the same timing scheme that was used for the single-cycle tests described earlier; only in this case, the six-bits of output information came from the up/down counter of the PLL.

The desired function of the loop is that it be able to take a raw Omega signal, such as the one depicted in Figure 9, and produce one number representing the true phase at the end of the measurement interval. If the loop time constant is too short, the loop will follow the phase closely and will yield bad data due to variations caused by impulse noise. Conversely, if the loop correlates over too many carrier cycles, the loop might not be able to keep up with the changes in phase due to aircraft motion.

One method of determining if the time constant of the loop is too short is to plot the histogram for the phase, since the shape of that curve determines the certainty that the phase number produced by the loop is accurate. Histograms

for various loop configurations are shown in Figures 19, 20, and 21 for the skipping of three, seven, and ten-bits respectively. The method of obtaining these graphs is the same as the one described in Chapter II, Section B. Again, a mathematical model of the phase distribution of a sinusoid in Gaussian noise is included as a reference. Although the phase distribution of the incoming phase is Laplacian, the Gaussian model is given since the algorithm defining its shape is defined in terms of signal-to-noise ratio. This allows for the analysis of the loop to be performed in more familiar terms (i.e., dB).

In Figure 19 the shape of the distribution has a considerably sharper peak than the distribution of the raw signal, and more closely approximates the mathematical model. However, the phase distribution still exhibits the characteristics of a signal affected by impulse noise. It is desirable that, in the final analysis, the output of the loop exhibit a Gaussian distribution, since the erratic variations caused by impulse noise would interfere with later processing of the phase information. If the phase distribution remained Laplacian, it would indicate that the phase was being perturbed in an impulse manner. A Gaussian distribution would be more desirable since, on the average, the probability that any one data point does not exceed an error threshold is greater than would be expected from a Laplacianly distributed phase. The above is most important in later processing. When the integration time of the loop is increased, as can be seen from Figures 17 and 18, the distribution of the loop output does approach a Gaussian distribution.

The signal-to-noise ratio numbers represented by the mathematical models in Figures 19, 20, and 21 are 4, 6, and 13 dB, respectively. Since equipment and processing limitations prevented this data from being accumulated at the same time,

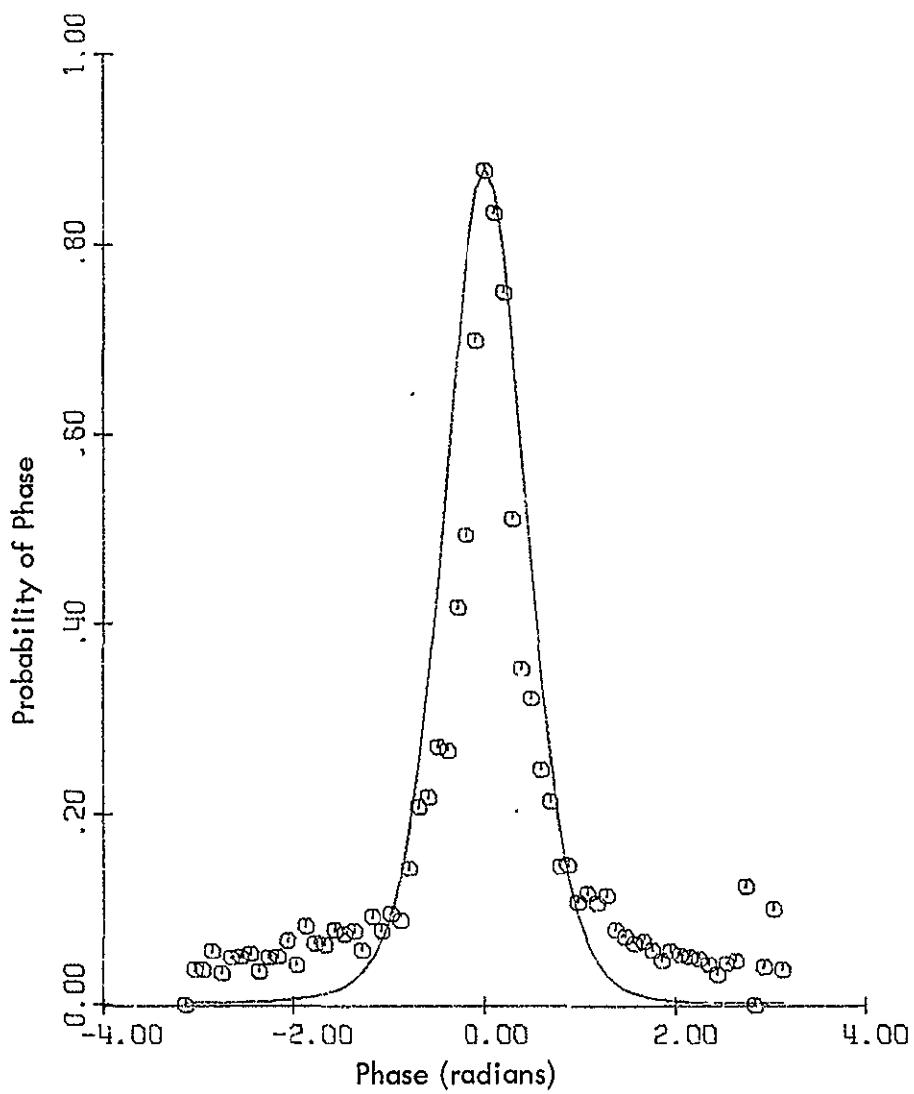


Figure 19. Phase Distribution for the Trinidad Station after 3 bits of Integration.

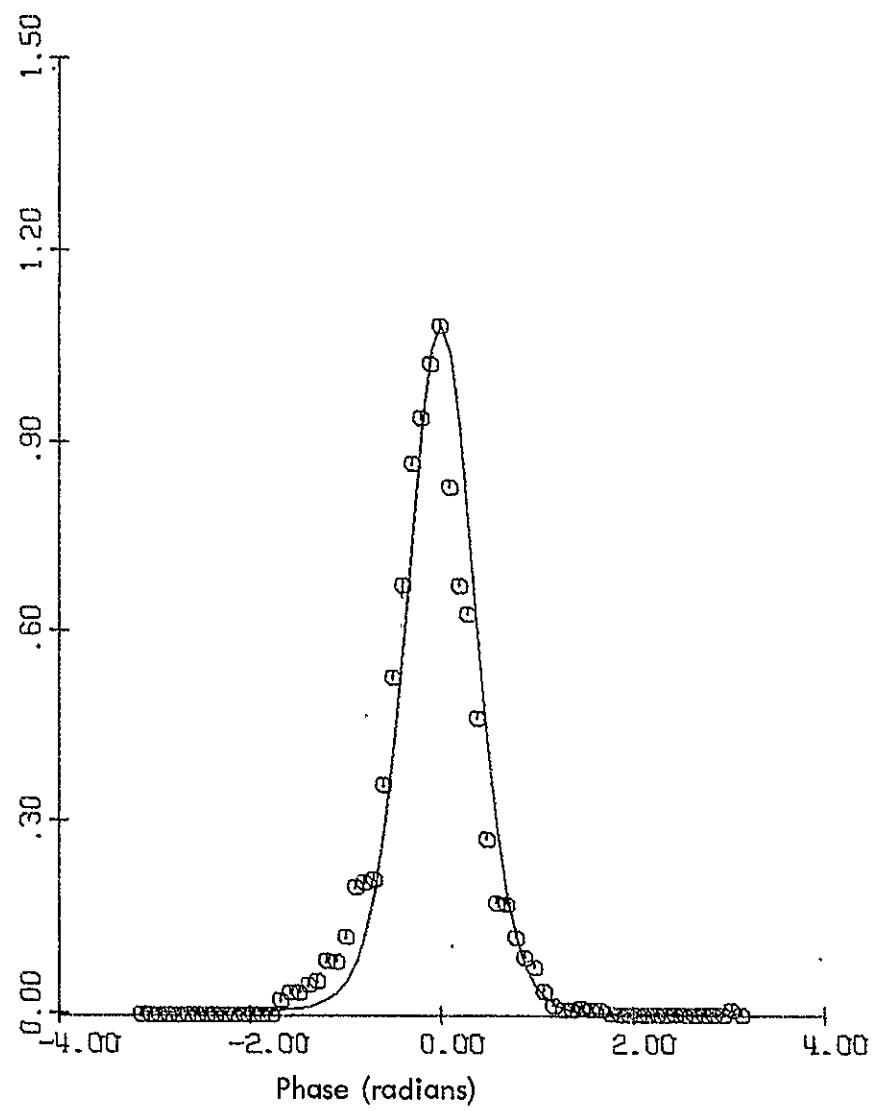


Figure 20. Phase Distribution of the Trinidad Station after 7 bits of Integration.

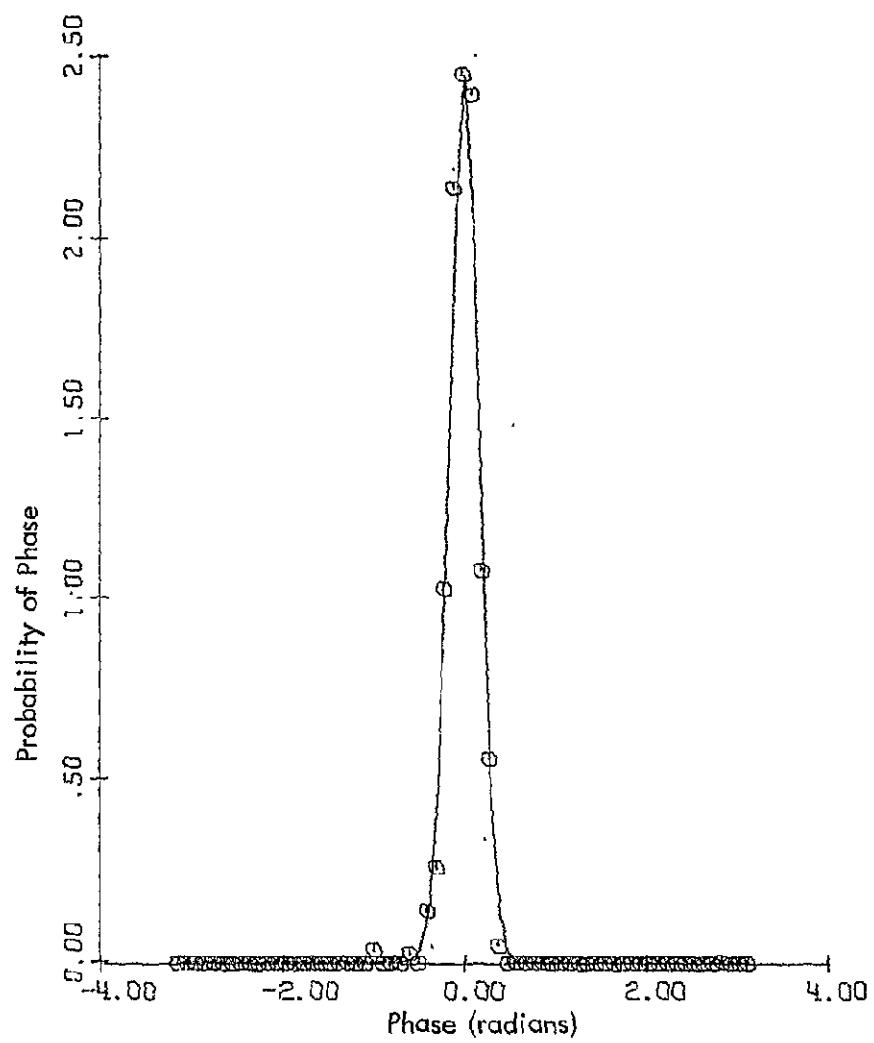


Figure 21. Phase Distribution of the Trinidad Station after 10 bits of Integration.

no attempt will be made to determine a signal-to-noise ratio improvement number for the loop. This is due to the fact that the nature of the noise changes quite radically within a short period of time, which would imply that the data would have to be taken simultaneously in order to make any statements about integration time and signal-to-noise ratio improvement. These numbers could easily be determined by repeating these tests using an Omega signal simulator to generate the incoming signals.

However, one conclusion that can be drawn from the data is that the signal-to-noise ratio does improve and the phase distribution does become more Gaussian with decreasing variance with increasing loop integration time.

The phase distribution of Figure 21 (the ten-bit integration case) appears adequate in that the probability of accuracy is high (the variance is small) and the shape is Gaussian. Yet, as mentioned, another constraint on the loop is that it be able to track the phase of an Omega signal while the loop is physically traveling at 200 miles/hour (or experiencing an equivalent rate of change of phase). Since the loop requires at least 1024 zero crossings to make a one-bit change (1/64th of a cycle) in phase, then in a 625 ms. measurement interval it can change by at most six-bits per time slot ( $(10.2 \times 10^3 \text{ cycles/sec} \times .625 \text{ sec/time slot})/1024 \text{ cycles/one-bit change} = 6 \text{ bits/time slot}$ ). Since the typical Omega lane width is about eight miles, six-bits (6/64ths of an Omega lane) represents .75 miles. Now, since the time slots are ten seconds apart, the loop can compensate for .75 miles in ten seconds or 270 miles/hour, which is well within the constraint placed on the loop.

As mentioned in this chapter, Section A, the phase detector will give a single output per cycle, regardless of how far displaced the locked signal and the Omega signal are. Therefore, the lock-up rate will be constant until the locked signal enters the skirt of the Omega phase distribution (see Figure 22) at which point the phase detector will start feeding some of the counts into the decrease phase line, thus slowing the lock rate. Since the greatest phase difference that the loop can experience on initial start-up is one-half cycle (since it can achieve lock bi-directionally), the longest time required to lock-up on the signal is six time slots or one minute.

The results contained in this section have been verified by a computer simulation [15] of this PLL configuration.

C. Memory-Aiding for Time Multiplexing. As mentioned in the previous section, the loop can change its locked phase by at most six-bits in the 625 ms. measurement interval. This limitation, although necessary for filtering, prohibits the use of one loop for measuring the phase of more than one Omega station. For instance, if the difference in phase between the North Dakota (D) and Trinidad (B) stations was ten-bits (10/64ths of a cycle), the loop would not be able to traverse the phase difference during the measurement intervals.

However, if the data obtained at the end of the previous measurement interval for that station were preset into the up/down counter at the beginning of the next measurement interval for that station, the loop could then accommodate all eight Omega time slots. This loop update is accomplished through the use of a random access memory (RAM), hence the time-multiplexed loop is referred to as the memory-aided phase lock loop (MAPLL). The block diagram for the MAPLL

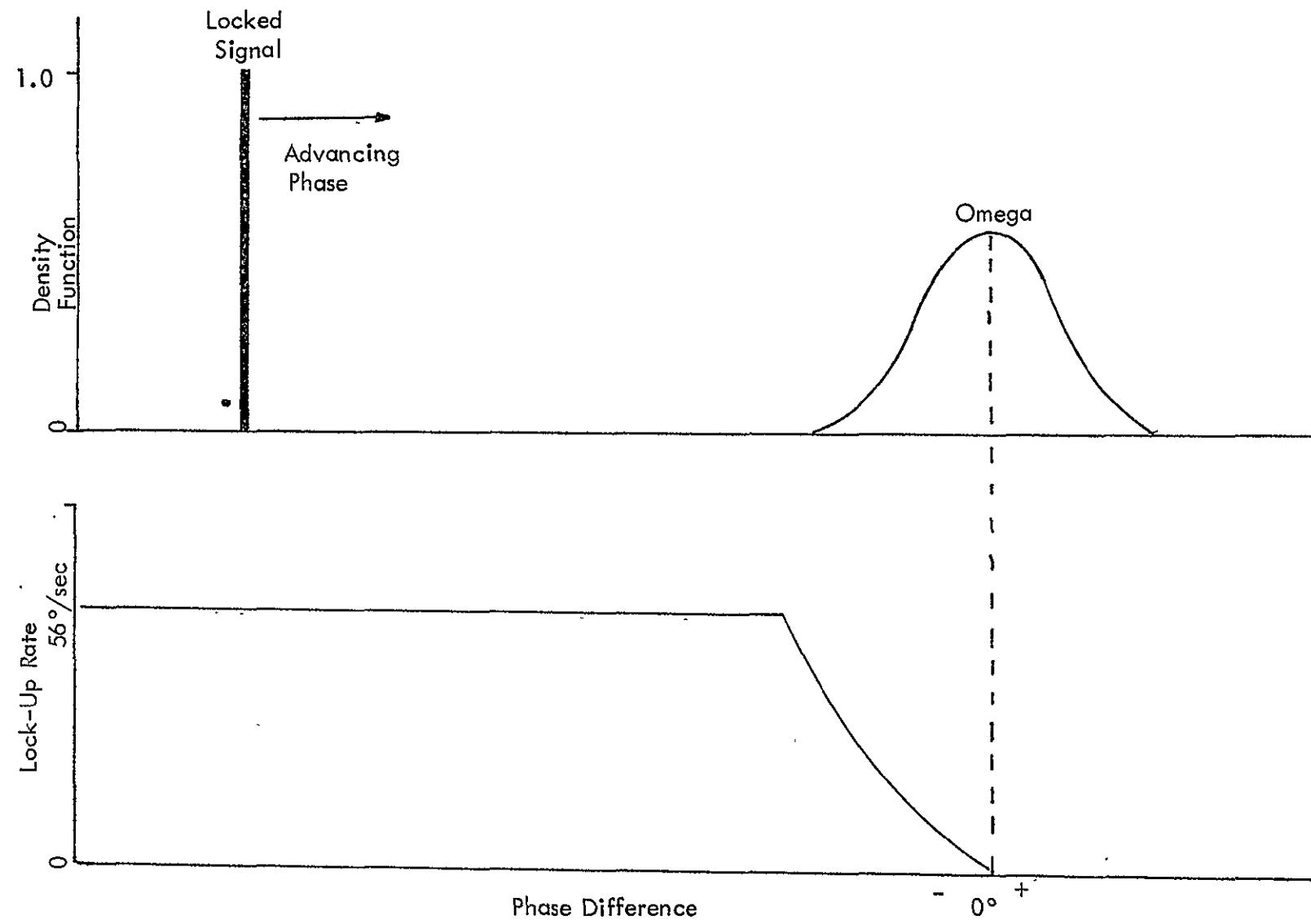


Figure 22. Lock-Up Rate versus Phase Difference.

is shown in Figure 23, which is similar to the DPLL shown in Figure 11 except that a RAM is connected to the loop with its output connected to the preset lines and its input connected to the control lines of the up/down counter.

Timing for the memory-aiding process is provided by the receiver timing circuit, known as the "housekeeping timer (HKT)". The HKT designates a three-bit address to each of the eight Omega time slots and feeds this address to the RAM. The timing scheme for the use of this memory is shown in Figure 24. Since this scheme represents one time slot, the three-bit address is constant for the 1.25 interval; therefore, all reading and writing operations in that interval are performed on the same memory location. Data for all eight Omega time slots is contained in a RAM, which not only allows for time-multiplexed loop operation, but creates a convenient digital interface. During each measurement interval, there is over 400 ms. that the memory is not used by the loop, so the RAM could be read and/or written by some peripheral device, such as a microprocessor, without interfering with the loop operation. If desired, a microprocessor could be used for velocity aiding by placing the expected value of phase for the next time slot into memory, i.e., creating a second order loop. This aspect for the MAPLL is discussed by Lilley<sup>[ 16 ]</sup>.

#### IV. CONCLUSIONS

The data generated by the PLL configuration described in this thesis is capable of providing good Omega data to a navigation processor. In fact, after hundreds of hours of data taking with the MAPLL and a commercially available

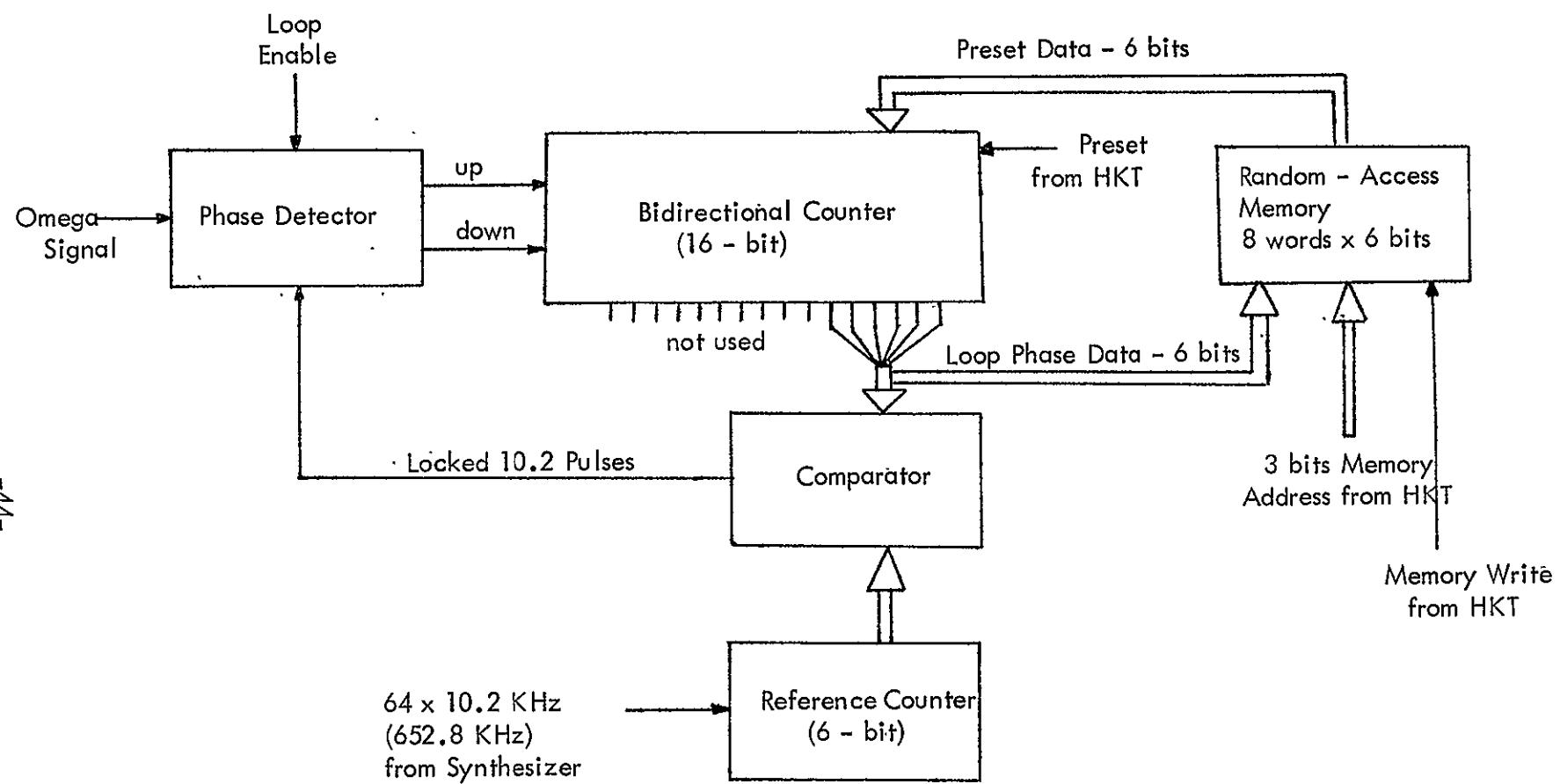


Figure 23. Memory-Aided Phase-Locked Loop (MAPLL).

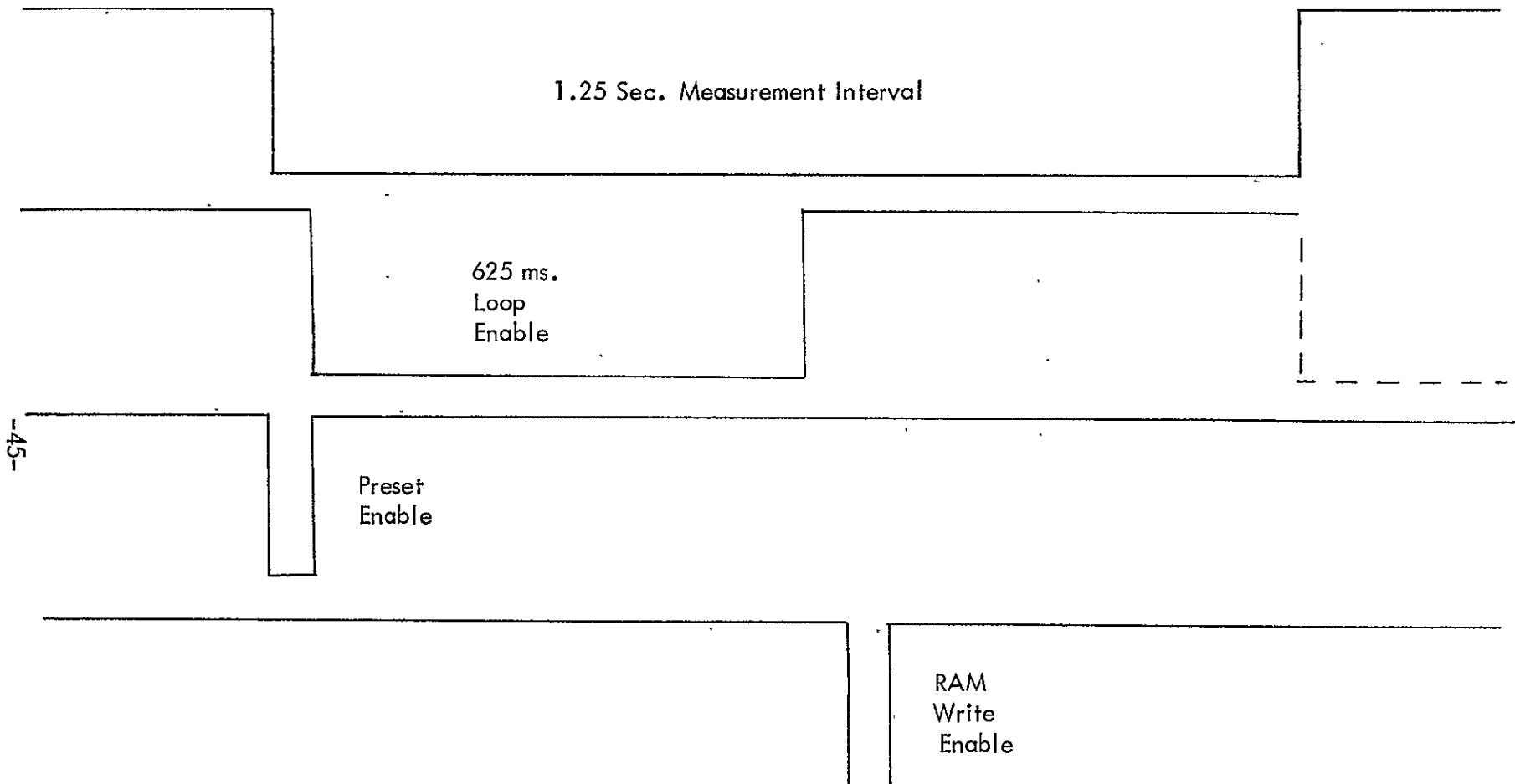


Figure 24. MAPLL Timing Sequence.

receiver (which has been referenced in the literature as being a standard), the MAPLL has consistently equalled or surpassed the commercial receiver in phase tracking ability.

The output of the MAPLL is an addressable six-bit binary number that represents the relative phase of any one of eight Omega stations. This data can be easily manipulated to generate hyperbolic lines of position (LOP's) with little additional logic (the current prototype receiver at the Avionics Engineering Center generates two analog LOP's with 2 D/A converters and 10 IC's). If greater sophistication is desired, such as a pilot-oriented display, diurnal corrections, or rate-aiding, a microprocessor can be interfaced to the MAPLL with little difficulty, since its outputs are digital and addressable.

The phase detector for the MAPLL, although extremely simple (employing only three logic gates), has proven itself over other more sophisticated phase detectors. The reason for its simplicity is that it is only required to make one decision per Omega carrier cycle. The benefit of such a scheme, aside from inexpensive implementation, is that it will not become disabled in a high noise environment and tends to be less susceptible to impulse noise.

The MAPLL has proven itself in more than just a laboratory environment. In fact, it has generated good sensor processor data (raw phase information) on several flight evaluations. An analysis of this flight data<sup>[ 17 ]</sup> has shown that the MAPLL compares well with other Omega sensor processors.

Although the MAPLL design is reasonably well-established, there are other circuit configurations based on the original MAPLL that should be suggested, such

as the implementation of CMOS, large scale integration (LSI), and rate-aiding. CMOS is a type of logic that uses much less power and is more noise immune than TTL logic. LSI, the feasibility of which is presently being ascertained, would allow the entire MAPLL to be placed on one integrated circuit. Rate-aiding, resulting in a second-order loop, would allow the MAPLL to be used on higher speed aircraft.

## V. ACKNOWLEDGEMENTS

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